B.TECH.

EEC 101

FIRST SEMESTER EXAMINATION 2010-11

ELECTRONICS ENGINEERING

Time: 3 Hours *Total Marks: 100*

Note: *(i) Attempt all questions. All questions carry equal marks. Assume any data, not given suitably.*

Section A

1. Attempt all the parts of this question. All parts of the question carry equal marks. These questions contain 10 objectives/fill in the blanks type/true-false type questions. (2 × 10 = 20)

(i) The knee voltage of a p-n junction is _____ after doping.

Ans. Constant

(ii) The Zener diode works as

(a) Current regulator

(b) Voltage regulator

(c) Power regulator

(d) Both (a) and (b)

Ans. (b) Voltage regulator

(iii) PIV of all the diodes of center-Tapped-transformer-full-wave-rectifier is

Ans. $2V_m$

(iv) The biasing circuit which gives best stability to the Q point is

(a) Base resistor biasing

(b) Emitter resistor biasing

(c) Potential divider biasing

(d) Feed back resistor biasing

Ans. (c) Potential divider biasing

(v) The parameters α and β of a bipolar junction transistor are related as _____.

Ans. $\beta = \frac{\alpha}{1-\alpha}$

(vi) The gate of a depletion type MOSFET is made up of

(a) metal

(b) semiconductor

(c) both

(d) none

Ans. (a) metal

(vii) The input impedance of a JFET is

(a) Very high

(b) Very low

(c) Moderately high

(d) Moderately low

Ans. (a) Very high

(viii) The DC Morgan's Theorem states that_____.

Ans. The whole complement of the product of a number of binary variables is equal to the sum of the individual complements of the same variables

$$\overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$$

(ix) The CRO can measure

(a) phase

(b) voltage

(c) current

(d) none of the above

Ans. (b) voltage

(x) **The full-scale deflection of ohm scale in a multimeter reads**

(a) Infinite resistance

(b) Zero resistance

(c) Some finite resistance

(d) none of the above

Ans. (b) Zero resistance

Section B

2. Attempt any three parts of the following: **(10 × 3 = 30)**

(a) Define and explain the following terms in respect of p-n junction.

(i) depletion layer

(ii) barrier potential,

(iii) AC and DC resistance,

(iv) Diffusion and transition capacitance,

(v) PIV,

(vi) ripple factor

Ans. (i) Depletion layer: The positive and the negative uncovered charges generate an electric field across the junction directed from the n-side to the p-side. This field opposes the diffusion of electrons and holes through the function. When equilibrium is reached there is no movement of charge carriers across the junction, the neighbourhood of the junction which is depleted of charge carriers is called deplection layer or region.

(ii) AC resistance: It is the slope of the volt-ampere characteristics. It is defined for small signal.

$$r = \frac{dV}{dI}, r = \frac{V_T}{I}, V_T = 26\ mV$$

DC resistance: It is the resistance offered by a diode to the dc current. It is also the ratio of dc voltage across the diode to direct current.

$$R = \frac{V}{I}$$

(iii) Barrier potential: The potential generated by the positive and the negative uncovered charges across the junction directed from the n-side to p-side which opposes the diffusion of electron and holes through the junction is barrier potential.

(iv) Diffusion capacitance: When the junction is forward biased, the potential barrier is reduced electrons and holes start entering p-side and n-side regions; thus the amount of stored charge varies with applied forward potential. This is called diffusion capacitance.

$$C_D = \frac{dQ}{dV} = \frac{\tau I}{\eta V_T}$$

Transition capacitance: A reverse bias causes more immobile charges to uncover, thus the thickness of depletion region increases with increase in reverse bias and vice versa. This increase/decrease in number of uncovered charges with applied reverse bias is called transition capacitance.

$$C_T = \left|\frac{dQ}{dV}\right|$$

(v) PIV: It is the peak voltage across the diode in the reverse direction i.e., when the diode is reverse biased eg. for Half wave rectifier PIV of each diode is V_m.

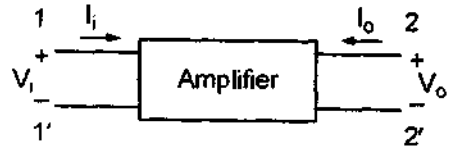
(vi) Ripple factor: The measure of ripples present in the output is by ripple factor.

Ripple factor

$$= \frac{\text{rms value of ac component in output}}{\text{average or dc component present in output}}$$

(b) Explain the h-parameter model of a Bipolar Junction Transistor.

Ans. h-parameter model:



$$V_i = f_1(I_i, V_o)$$
$$I_i = f_2(I_i, V_o)$$

$$\begin{bmatrix} V_i^o \\ I_o \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_i^o \\ V_o \end{bmatrix}$$

$\Rightarrow$

$$V_i^o = h_{11} I_i^o + h_{12} V_o$$

$$I_o = h_{21} I_i^o + h_{22} V_o$$

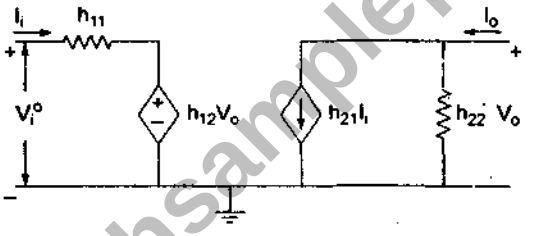
$$h_i^o = h_{11} = \left.\frac{V_i^o}{I_i^o}\right|_{V_o = 0}$$ = Input resistance with output S.C.

$$h_r = h_{12} = \left.\frac{V_i^o}{V_o}\right|_{I_i^o = 0}$$ = Reverse transfer voltage ratio with input O.C

$$h_f = h_{21} = \left.\frac{I_o}{I_i^o}\right|_{V_o = 0}$$ = Forward current transfer ratio with output S.C

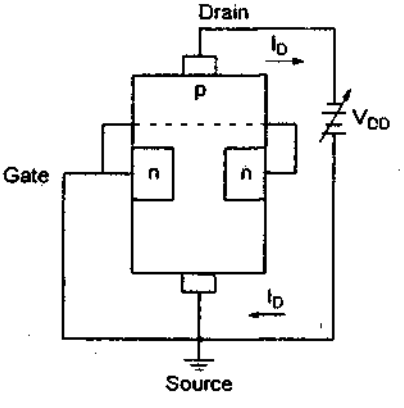
$$h_o = h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i^o = 0}$$ = Output admittance with input O.C.

h-model



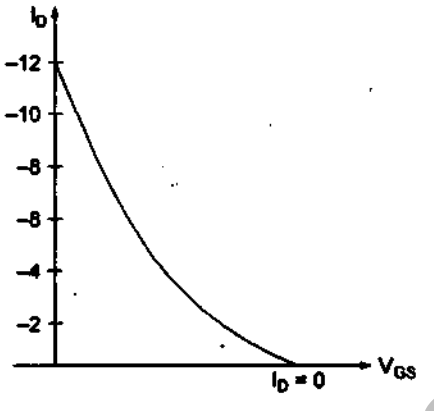
(c) Explain the working of p-channel JFET. Draw the I_D vs V_{DS} of the following circuit.

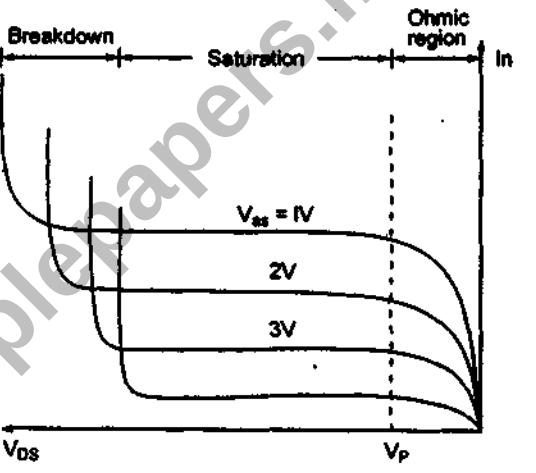
Ans. p-channel JFET: Small bar of extrinsic semiconductor material p-type is taken. At the two ends, two ohmic contacts are made i.e., drain and source. Heavily doped electrodes of '*n*' type form the p-n junction on each side of the bar. The region between the two p-n junction is called channel.



- In the absence of any applied potential, a depletion region is at each junction.

- When $V_{GS} = 0$ and $V_{DS}(V_{DD})$ is small (–ve) voltage, the holes from source side are pushed towards the channel, thus establishing the current 'I_D'.
- The holes move from source and drained out from drain.
- When V_{DS} is further increased, since the p-type bar has uniform resistance, I_D causes a voltage drop across this resistance i.e., in the channel. The reverse bias between gate and channel increases thereby increasing the depletion region more in the channel rather than in gate. A stage will come when I_D becomes constant as channel width is reduced to very small opening. This pt is called pinch off.
- When reverse bias is applied between gate and source, the depletion region is further increased and the channel is closed, reducing the current to zero, this is called cut off gate to source voltage.





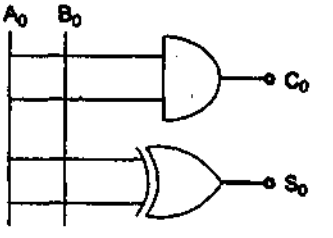
(d) Draw and explain the binary half-adder and half-subtractor circuits. How they are used to work as full adder and full subtractor circuits?

Ans. Half Adder:

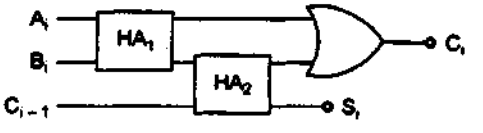
$S_o = A\bar{B} + \bar{A}B = A \oplus B$

$C_o = AB$

Input		Output	
B_o	A_o	Sum (S_o)	Carry (C_o)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Full Adder using Half Adder

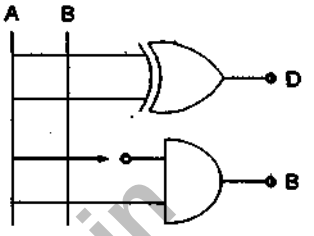


Half Subtractor

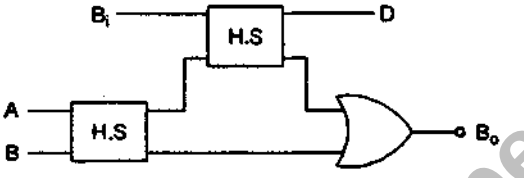
$D = \bar{A}B + A\bar{B}$

$B = \bar{A} \cdot B$

Input		Output	
B	*A*	Difference (D)	Borrow (B)
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0

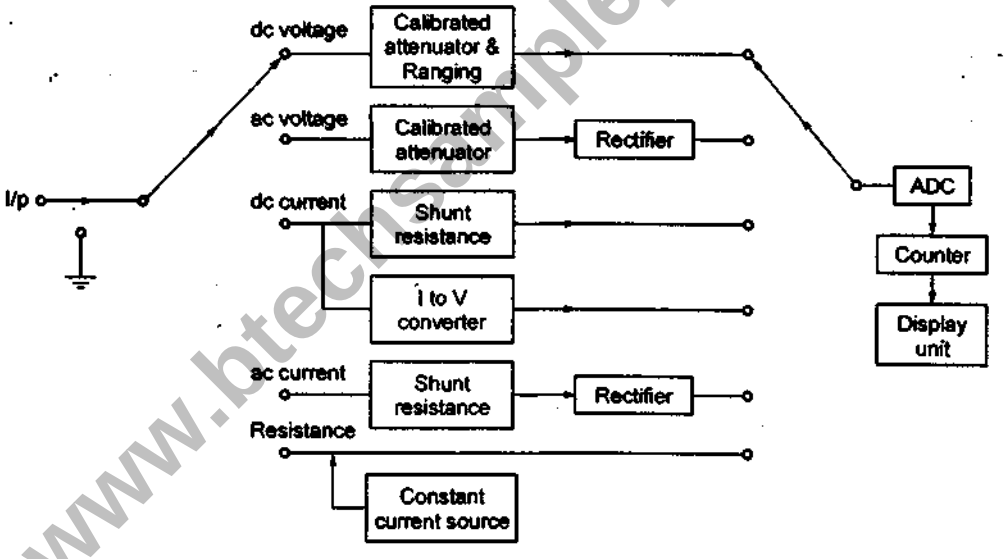


Full subtractor:



(e) With the help of block diagram explain the working of digital multimeter. What are the characteristics of Digital Voltmeter used in a typical digital multimeter?

Ans. Digital Multimeter:



- The multimeter is used to measure ac, dc currents and voltages and also used to measure resistance.
- The dc voltage is passed calibrated attenuator so as to being it within the range of instrument. The output from attenuator is passed through Analog to Digital Converter (ADC). The digital output is counted by counter and shown by display unit. The displayed value is the input dc voltage applied at the input side.
- Similarly ac voltage is passed through attenuator and then through ac to dc Convertor or Rectifier and then *ADC* counter and display.

- AC current and DC current are also measured in similar way but this is first converted to voltage using either shunt resistance or current to voltage coverter.
- Resistance is measured with the help of constant current source, which develops a potential. The displayed value is prop. to resistance to be measured.

Characteristics of digital voltmeter:

(i) Number of measurement ranges

(ii) Number of digits in read out

(iii) Accuracy

(iv) Speed of the reading

(v) Normal mode noise rejection

(vi) Common mode noise rejection

(vii) Digital output of several types

(viii) Input impedance

Section C

Note: Attempt all the questions. All questions carry equal marks. (10 × 5 = 50)

3. Attempt any two parts of the following. (5 × 2 = 10)

(a) Show that the maximum efficiency of Half wave rectifier is 40.6%.

Ans. Half wave Rectifier: Ratio of dc power to input ac power is efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{Im^2}{\pi^2}\right) \cdot R_L}{\frac{I_m^2}{4}(R_f + R_S + R_L)}$$

$$= \frac{\left(\frac{4}{\pi^2}\right) R_L}{R_f + R_L + R_S} = \frac{0.406}{1 + \left(\frac{R_f + R_S}{R_L}\right)}$$

If $R_f + R_S << R_L$ then

η = 0.406 or 40.6%

(b) An ac voltage of peak value 20V is connected in series with a Si diode and load resistance of 1 KΩ. If the forward resistance of diode is 15 Ω find

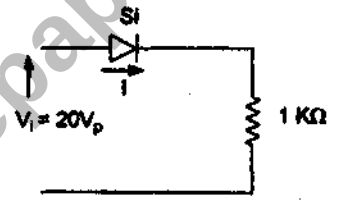
(i) peak current through diode

(ii) peak output voltage.

Ans. $r_f = 15\ \Omega$, $R_L = 1\ K\Omega$ $V_\gamma = 0.7$ V

(i) Peak current, $I = \frac{20 - 0.7}{1000 + 15}$

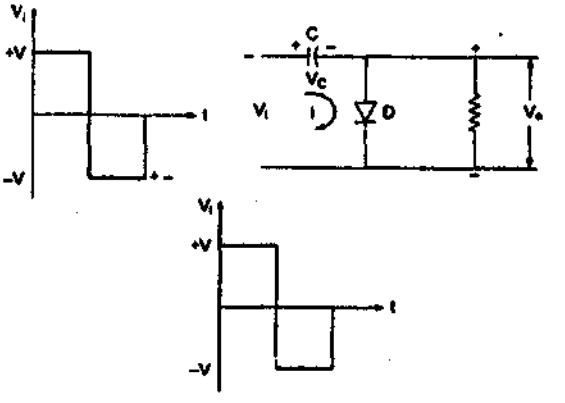
$= \frac{19.3}{1015} = 0.0190A = 19$ mA.



(ii) Peak output voltage = 20 – 0.7 = 19.3 V

(c) Describe the working of clamping circuit with neat diagrams.

Ans. Clamper: For +ve cycle of input diode '*D*' is forward biased and capacitor starts charging to peak value of input i.e., *V*.



Hence voltage across $V_C = V$ capacitor

Output voltage, $V_o = 0$V.

For –ve cycle of input diode 'D' is reverse biased and is off, thus the capacitor will act as source for current to the load.

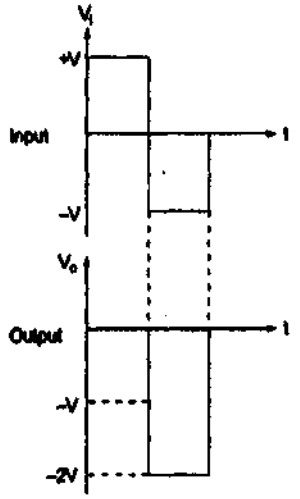
Thus output voltage can be calculated as

$$-V_c - V_o - V = 0$$

$$\therefore \quad V_o = -V_c - V$$

$$= -V - V$$

$$\boxed{V_o = -2V}$$



4. Attempt any one part of the following: **(10 × 1 = 10)**

(a) (i) In a CE transistor amplifier circuit, V_{CE} is increased from 2 to 12 V, the collector current changes from 3 to 4 mA, determine the output resistance.

Ans. Output resistance $= \dfrac{12-2}{(4-3)\times 10^{-3}}$

$$= \frac{10}{1\times 10^{-3}} = 10\ \text{K}\Omega$$

(ii) In an n-p-n transistor $\alpha = 0.98$, I_E = 10mA. leakage current I_{CBO} = 1μA. Determine I_C, I_B, β, I_{CEO}.

Ans. $\alpha = 0.98$, $I_E = 10$ mA $I_{CBO} = 1$ μA

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \frac{0.98}{0.02} = 49$$

$$\alpha = \frac{I_C}{I_E}$$

$$\Rightarrow \quad I_C = \alpha I_E = 0.98 \times 10 = 9.8\ \text{mA}$$

$$\beta = \frac{I_C}{I_B}$$

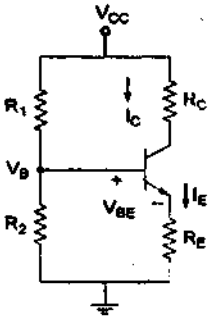
$$\Rightarrow \quad I_B = \frac{I_C}{\beta} = \frac{9.8}{49} = 0.2\ \text{mA}$$

$$I_{CEO} = (1+\beta) I_{CBO} = (1+49) \times 1 = 50\ \mu\text{A}.$$

(b) Why biasing is needed in a BJT? Which of the biasing circuit is most preferred and why? Explain in detail.

Ans. For most of the application, transistors are required to operate as linear amplifier. This can be achieved by operating the transistor over region of its characteristics curve which are linear, parallel and equispaced for equal increments of parameter. In order to operate in desired regions external dc voltages of correct polarity and magnitude to two junctions are necessary. That is why biasing is required.

Potential divider bias is generally used as it gives stable Q-pt against changes in parameters.



In the circuit R_1 and R_2 act as potential divider giving a fixed voltage V_B at the base.

If I_C increases due to change in temperature or 'β', I_E also increases and thus voltage drop across R_E also increases, this reduces the voltage difference between base and emitter i.e., V_{BE}. Due to reduction in V_{BE}, I_B will also decrease and this results in decrease in I_C.

This shows that (–ve) feedback results in emitter bias or potential divider bias, which compensates for any change in I_C.

5. Attempt any one part nf the following.

(10 × I = 10)

(a) Explain the characteristics of an ideal operational amplifier. Sketch nnity gain amplifier and non-inverting amplifier and find the output vnltages In terms of Input voltage. Explain why the operatinnal amplifier is called nperational amplifier?

Ans. Ideal operational amplifier:

(i) Infinite gain

(ii) Infinite input impedance

(iii) Zero output impedance

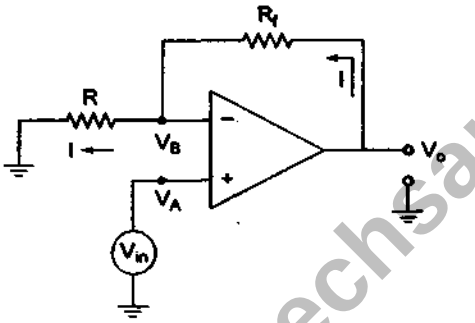
(iv) Infinite slow rate

(v) Infinite CMRR

(vi) Infinite Bandwidth

(vii) No effect of temperature

(viii) Zero offset voltages



Non Inverting Amplifier

$$V_A = v_{in}$$

Due to virtual ground concept

$$V_B = V_A = v_{in}$$

Applying KCL from output side

$$\frac{V_O - V_B}{R_f} = \frac{V_B - R}{I}$$

$$\frac{v_o - v_{in}}{R_f} = \frac{v_{in}}{R} \quad (v_B = v_{in})$$

$$v_{in}\left[\frac{1}{R} + \frac{1}{R_f}\right] = \frac{v_o}{R_f}$$

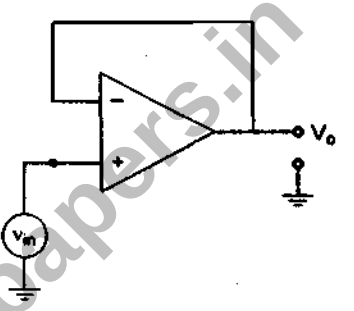
$$\therefore \quad \boxed{v_o = \left(1 + \frac{R_f}{f}\right) v_{in}}$$

Unity Gain Amplifier

If in noninverting amplifier $R_f = 0$ and $R = \infty$, then

$$v_o = \left(1 + \frac{0}{\infty}\right) v_{in}$$

$$\boxed{v_0 = v_{in}}$$



Operational Amplifier: Operational amplifier can perform various mathematical operations like addition, subtraction, integration, differentiation, etc and also it can amplify ac as well as dc signals, it is named operational amplifier.

(b) Explain pinch nff voltage, maximnm satnration snurce current and transconductance of a FET. A FET has the transconductance of 3500×10^{-6} **mho and the load resistance is 10 KΩ and is used in voltage amplifier eircult. Calculate the voltage amplificatinn assnming that** $r_d >> R_1$.

Ans. Pinch off voltage: The voltage V_{DS} at which current I_D reaches to its constant saturation value keeping $V_{as} = 0$ is called pinch off voltage.

Max. saturation source current: When no gate to source voltage is applied ($V_{GS} = 0$) and depletion width is minimum of *p–nj"* in FET, the width of conducting channel is maximum, I_D is maximum, this is the maximum saturation current.

Transconductance:

It is the change in the I_D for given change in V_{GS} with V_{DS} = constant.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ =\ \text{constant}}$$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS\ off}}\right]$$

or $$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right].$$

Given $g_m = 3500 \times 10^{-6}$ mho

$R_d = 10\ K\Omega$ $\mu = ?$

$\mu = R_d \times g_m$

$= 10 \times 10^3 \times 3500 \times 10^{-6}$

$\boxed{\mu = 35}$

6. Attempt any two parts of the following: **(5 × 2 = 10)**

(a) Whether the following expressions are true of false? State the theorems used.

(i) $AB + ABC + A'B = AB'C = B + AC$

Ans. Taking L.H.S $AB[1 + C] + A'B + AB'C$

$1 + C = 1 \rightarrow$ OR Law

$\Rightarrow AB + A'B + AB'C$

$\Rightarrow A[B + B'C] + A'B$ $B + B'C = (B + B')(B + C)$ Distributive property

$\Rightarrow A[B + C] + A'B$

$\Rightarrow AB + AC + A'B$

$\Rightarrow B[A + A'] + AC$ $A + A' = 1 \rightarrow$ Complement law.

$\Rightarrow B + AC$ = R.H.S.

(ii) $AB + AC + BC' = AC + BC'$

Ans. $AB + AC + BC' = AC + BC'$

Taking R.H.S $AC + BC'$

$\Rightarrow A(B + B')C + BC'$ $B + B' = 1$

$\Rightarrow ABC + AB'C + BC'$ (Complement law)

$\Rightarrow B[AC + C'] + AB'C\,AC + C' = (A + C')(C + C')$

$\Rightarrow B[A + C'] + AB'C$ Distributive law

$\Rightarrow AB + BC' + AB'C$

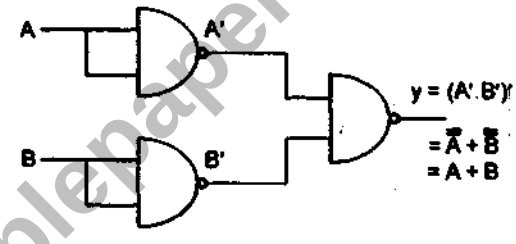
$\Rightarrow A[B + B'C] + BC'$ $B + B'C = (B + B')(B + C)$

$\Rightarrow A[B + C] + BC'$ Distributive law

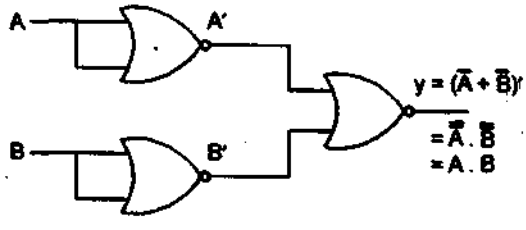
$\Rightarrow AB + AC + BC'$ = L.H.S.

(b) Realize OR gate using NAND gates only and gate using NOR gates only. Explain your answer.

Ans. OR from NAND



AND from NOR



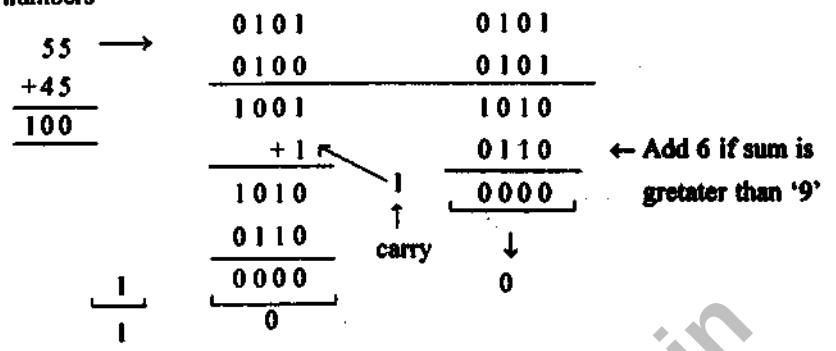
(c) Explain the BCD numbers. How two BCD numbers are added?

Ans. BCD members: When every digit of a decimal number is replaced by a nibble of binary it is called BCD numbers.

For example: 645 (decimal number)

= (01100100 0101) BCD.

Addition of BCD numbers



∴ 55 + 45 = 100 in BCD it is (0001 00000000)

7. Attempt any one part of the following: **(10 × 1 = 10)**

(a) Write the names of Non-Integrating and integrating type Digital Voltmeter. With the help of Block Diagram explain the working principle of any one of Integrating type DVM. Also give the merit and demerit of technique used.

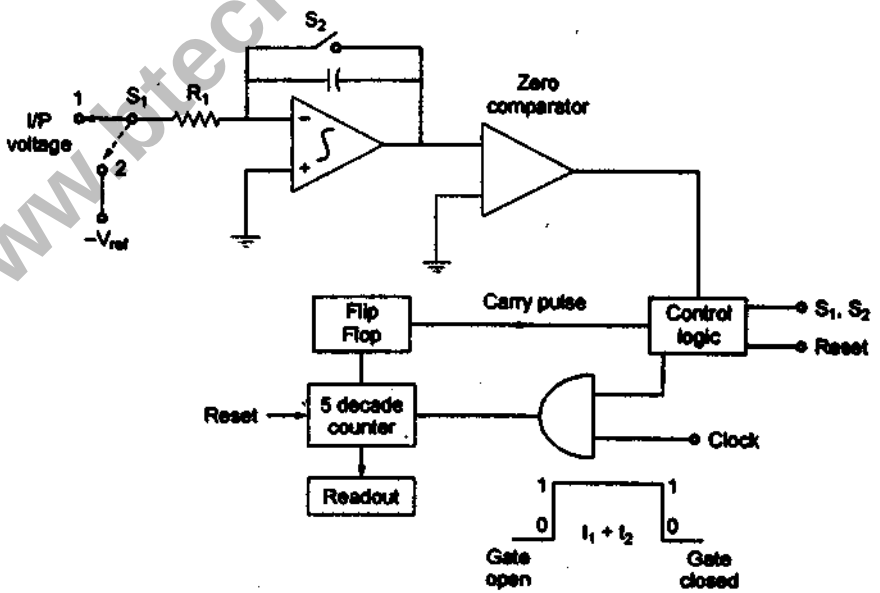
Ans. Non Integrating DVM

(i) Single slop DVM
(ii) Successive Approximation
(iii) Flash type
(iv) Servo potentiometric type
(v) Linear Ramp type
(vi) Staircase Ramp type

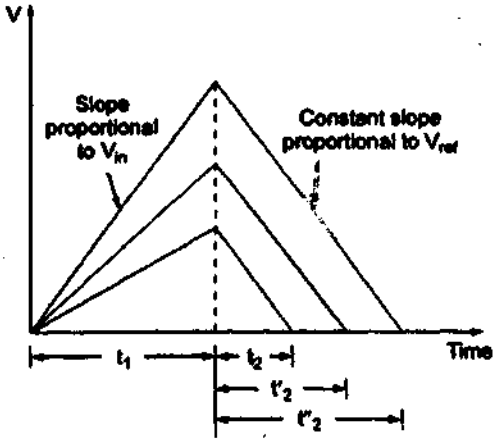
Integrating DVM

(i) Dual slope DVM
(ii) Voltage of frequency converter type
(iii) Potentiometric type

Integrating type: Dual slope type



At the start of the measurement the counter is resettled to zero. The output of the flip flop is also zero. This is given to the control logic. This control sends a signal to close S_1 to '1' position and thus integration of the input voltage starts. It continues till the time period 't_1'. As the output of the integrator changes from its zero value, the zero comparator output changes its state. The provides a signal to control logic which inturn opens the gate and the counting of the clock pulses starts.



The counter counts the pulses and when it reaches to 9999, it generates a carry pulse and all digits go to zero. The flip flop output gets activated to the logic level '1'. This activates the control logic. This sends a signal which changes the switch S_1 position from 1 to 2.

Thus v_{ref} gets connected to integrator. As v_{ref} polarity is opposite, the capacitor starts discharging. The integrator output will have constant negative slope. The output decreases linearly and after 't_2' capacitor gets fully discharged. At this instant the output of zero comparator changes its state. This inturn sends a signal to the control logic and gate gets closed. Thus gate is open for $t_1 + t_2$. The counting stops at this instant, the pulses counted by the counter have direct relation with input voltage.

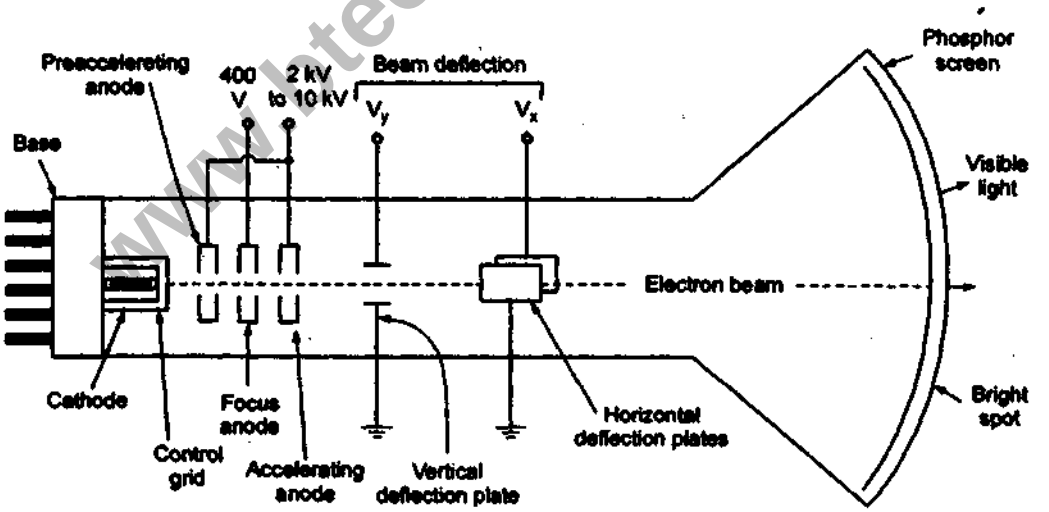
n_2 = digital count during gt_2.

n_1 = digital count during gt_1.

$$V_{in} = v_{ref} \cdot \frac{n_2}{n_1}$$

(b) Sketch a Cathode Ray tube used in a CRO and determine how many cycles of a 2-KHz sinusoidal are viewed if the sweep frequency is: 1 KHz, 2KHz, 4 KHz.

Ans. CRT



Signal freq. = 2 Khz (i) Sampling freq = 1 Khz.

(i) Sampling period $= \frac{1}{\text{Sampling freq}} = \frac{1}{1 \times 10^3} = 10^{-3}$ sec.

$\therefore$ Time period of sampling $= \frac{\text{no. of cycles}}{\text{Signal freq}}$

no. of cycle = Sampling period × Signal freq.

$= 10^{-3} \times 2 \times 10^3 = 2$ cycles.

(ii) no. of cycle $= \frac{1}{\text{Sampling freq.}} \times$ Signal freq.

Sampling freq = 2 khz.

$\therefore$ no. of cycle $= \frac{1}{2 \times 10^3} \times 2 \times 10^3 = 1$ cycle

(iii) Sampling frequency = 4 khz.

no. of cycle $= \frac{1}{4 \times 10^3} \times 2 \times 10^3 = \frac{1}{2}$ or half cycle.