B.Tech.

FIRST ODD SEMESTER THEORY EXAMINATION, 2009-10

ELECTRONICS ENGINEERING

(EEC-101)

Time : 3 Hours] *[Total Marks : 100*

Note : *(1) Attempt* ***all*** *questions.*

SECTION - A

Q. 1. Attempt all parts of this question. All parts of this question carry equal marks. This quastion contains TEN objective/Fill in the blank type/True Faise type questions: $2 \times 10 = 20$

Q. 1. (i) Whan PN-junction is biasad in the forward direction _____ in eacb region are injected into tha otber region.

Ans. electron hole.

Q. 1. (ii) In a centre-tap full-wave rectifier, V_m is the peak voltage between the centre-tap and one end of the secondary. The PIV of tha non conducting diode is _____ wben tbe filter is not connected.

Ans. 2 Vm.

Q. 1. (iii) Whicb os the following ststement is best suited for a Zener diode ?

(a) It is rectifiar diode.

(h) It works in tha forward hias region.

(c) It is a constant voltage device.

(d) It is mostly used in clipping circuit.

Ans. (c) It is a constant voltage device.

Q. 1. (iv) An ordinary transistor is cslied 'hipolar junction transistor' because it bas two poles : one positive and otber nagative. (True/False)

Ans. False.

Q. 1. (v) A common emitter transistor amplifier bas a gain of 150. The output voltage is measured as 2V AC, the input voltage will be _____.

Ans. $\frac{V_0}{V_{in}} = -150$, here $V_0 = 2V$

$$V_{in} = -\frac{V_0}{150} = -\frac{2}{150} = -1.33 \text{ Vott}$$

Q. 1. (vi) W The operation of JFET involves.

(a) a flow of minority carriers.

(b) A flow of majority carriers.

(c) Recombination.

(d) Negative resistance.

Ans. (b) A flow of majority csrriers.

Q. 1. (vii) An ideal operational amplifier is used to make an invarting amplifier. Thare are two input terminais of tbe operational amplifier and are at the same potential because :

(a) tbe two inputs are directly sbort circuitad internally.

(h) the input resistance of the operational amplifier is infinity.

(c) tbe open loop gain of tbe operational amplifier is infinity.

(d) all the above except option (a).

Ans. (d) all the above except option (a).

Q. 1. (viii) Tba α and β of a transistor are 0.99 and 99 respectively. If its I_{CBO} is 0.1 A, than its I_{CEO} will he

Ans. $I_{CEO} = I_{CBO}(1 + \beta)$

$= 0.1(1 + 99)$

$I_{CEO} = 10$ Amp.

Q. 1. (ix) A basic meter can be converted in to an ohmmeter by connecting :

(a) a variable resistance in series.

(b) a battery in series.

(c) Both (a) and (b)

(d) None of the above

Ans. (d) None of the above.

Q. 1. (x) $A + A'B =$

(ii) $A.(A' + B) =$

Ans. (i) $A + A'B = (A + A').(A + B)$

$[\because A + A' = 1]$

$\therefore \quad = (A + B)$

(ii) $A.(A' + B) = A.A' + AB \quad [\because AA' = 0]$

$= 0 + AB$

$= AB$

SECTION - B

Q. 2. Attempt any three parts of this question. All parts of this question carry equal marks : $10 \times 3 = 30$

Q. 2. (a) (i) Differentiate between static and dynamic resistance of a diode. **2**

Ans. (i) DC. or Static Resistance : It is the resistance offered by diode to the direct current.

At any point the D.C. or static resistance,

$$R = \frac{V}{I}$$

AC or Dynamic Resistance : It is resistance offered by diode to the changing forward current.

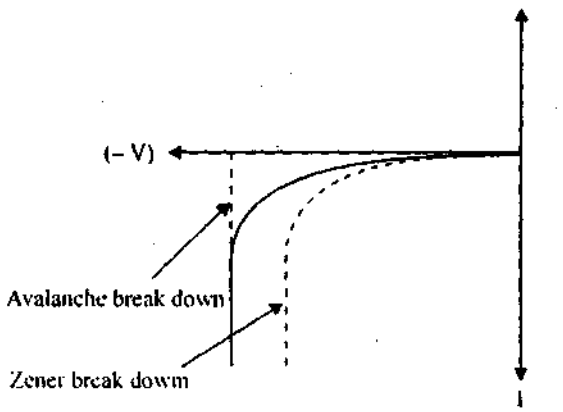
AC. or Dynamic Resistance,

$$r = \frac{\text{Small Change in forward voltage}}{\text{Small Change in forward current}} = \frac{\Delta V}{\Delta I}$$

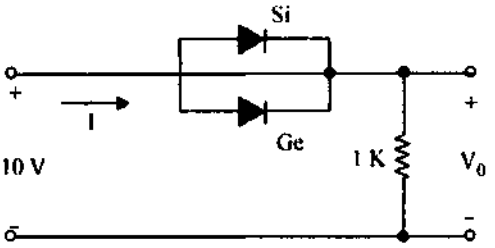
Q. 2. (a) (ii) Explain the two break down mechanisms of a reverse bias diode. **4**

Ans. Avalanche Breakdown : When the electric field becomes large enough so that the electrons moving in the depletion region gain enough energy b/w collisions to ionize neutral atoms. One mobile electron produces an additional second mobile electron and both carriers are capable of repeating the ionization process with new atoms. This phenomenon may be called avalanche multiplication of charge carriers. This result is rapid increase of current at the critical voltage level. This is also known as avalanche breakdown of the P.N Junction.

Zener Breakdown : Heavily doped P and n type regions on both sides of a P - N junction produce a very thin depletion region. Due to this electric field intensity in this region becomes so high, and electron are from their covalent bonds, which result into dislodge of great many electrons. From the valence bond in the depletion region and forces them across the boundary. This is called Zener effect. Which is responsible for large increase of current at the Critical Voltage.



Q. 2. a (iii) Determine V_0 and I for the following circuit. **4**



Ans. Due to short circuit of both diode are uneffective so $V_0 = 10$ V.

and $I = \frac{V_0}{1} = \frac{10}{1} = 10$ mA.

Q. 2. (h) (i) Which of the transistor currents is always the largest ? Which one is the smallest ? Which two are relatively close in magnitude ? **5**

Ans. When emitter junction forward biased most of the electrons injected from the emitter junction to the base (may be 99% or more) reach the collector junction, they came under the influence of the space charge region of the collector junction, so are swept into the collector region and then continue to flow as normal majority carrier current in the n-type material of the collector. This is the collector current I_c.

A small part of the electronic current from the emitter I_E is lost in the base due to recombinations. Some holes from the base region are consumed in that recombinations. To take the place of the holes lost in this way equal amount of holes must come to the baseregion fcom the base terminal outside. This constitute the base current I_B.

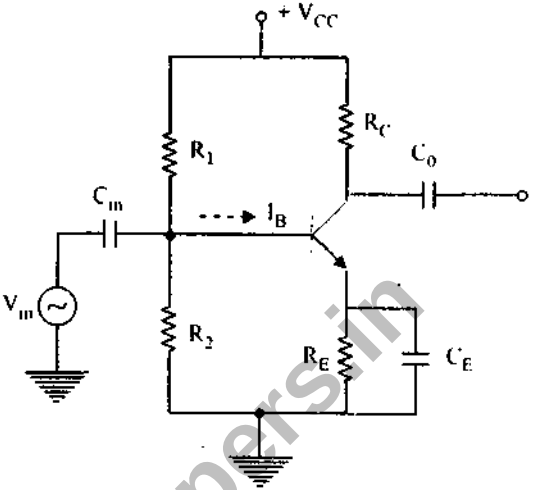
Thus, $\boxed{I_E = I_C + I_B}$

So the largest current will be I_E (99%) and smallest current will be I_B (2 to 5%).

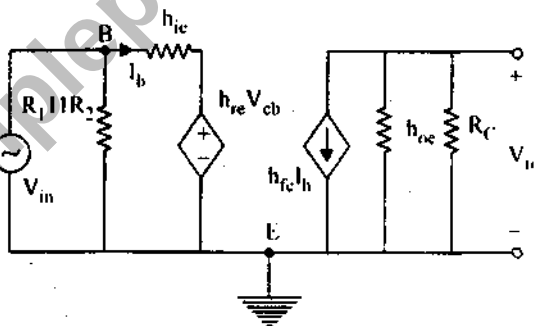
Hence, $I_E \approx I_C$.

Q. 2. (h) (ii) Draw the small signal equivalent circuit of a BJT and explain each component. **5**

Ans. For small signal (For frequency) model all coupling (C_{in}, Co) and bypass capacitor C_E, behave as short circuit.



Hence its equivalent circuit is



Here h_{ie} : Input Impedance of common emitter

h_{fe} : Forwor current gain.

h_{re}: Reverse voltage gain

h_{oe} : output admittance.

Q. 2. (c) (i) Define the following : **10**

(1) Drain to source saturation current of JFET.

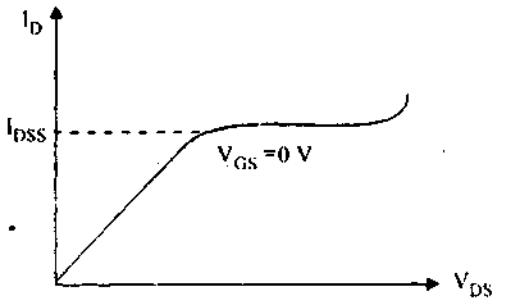
(2) Pinch off voltage of JFET.

(3) Voltage controlled resistance of JFET.

(4) Virtual ground in an op-amp.

(5) Voltage gain of a non-inverting amplifier.

Ans. (1) From shokley, equation,



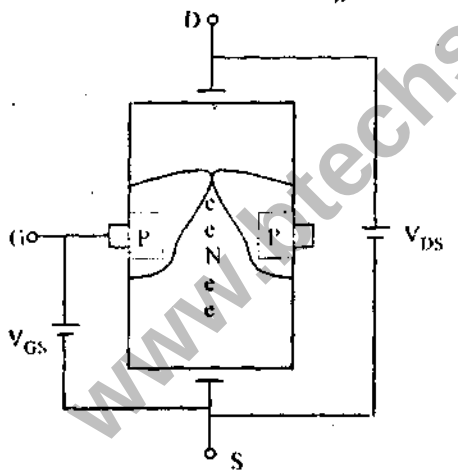
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

When gate to source voltage V_{GS} is zero then, $I_D = I_{DSS}$,

where I_{DSS} : Drain to source saturation current. It is maximum current attained by JFET when V_{GS} is zero.

(2) Pinch off voltage

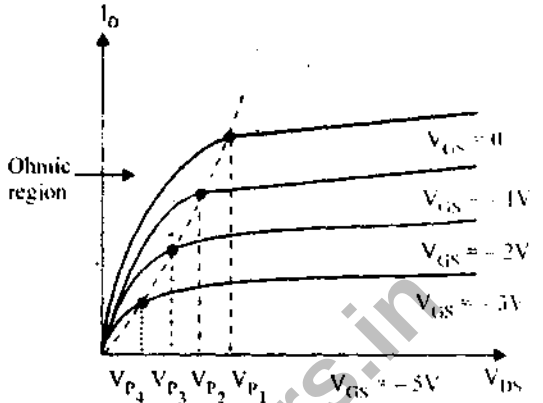
A minimum gate to source voltage (V_{GS}) at which drain current is zero *i.e.* ($I_D = 0$) is known as pinche off voltage $V_{GS(off)}$ or V_P



(3) Voltage controlled resistance of JFET

From *IV* characteristics of JFET,

In ohmic region it can be observed that as V_{GS} increases the slope of the current curve decrease, that mean the resistance of the channel increases. Hence the device can be

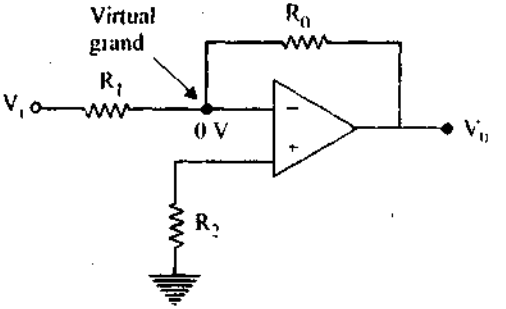


used in this region as a voltage controlled resistor. The resistance r,

$$r = \frac{v_0}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

(4) Virtual ground in an OP-amp :

Virtual ground is defined in an op-amp, as the other of its input terminal assuming ground potential automatically through feedback path when one of its terminal is connected to ground.



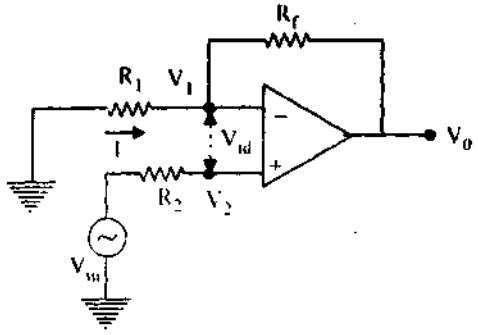
(5) Non-inverting amplifier :

$\because$ $V_2 = V_{in}$, but $V_1 = V_2 = V_{in}$

but $\frac{0 - v_1}{R_1} = \frac{v_1 - v_0}{R_F}$

$$\frac{V_0}{R_F} = \frac{V_1}{R_F} + \frac{V_1}{R_1}$$

$$\frac{V_0}{R_F} = V_{in}\left(\frac{1}{R_F} + \frac{1}{R_1}\right)$$



Gain of amplifier

$$Ac = \frac{V_0}{V_{in}} = \left(1 + \frac{R_F}{R_1}\right)$$

Q. 2. (d) (i) Prove the following identity 5

$$(x_1 + x_2).(x'_1 . x'_3 + x_3).(x'_2 x_1 . x_3)' = x'_1 . x_2$$

Ans.

$\Rightarrow$

$$(x_1 + x'_1 . x'_3 + x_1 x_3 + x_2 x'_1 x'_3)(x''_2 + x_1' + x_3') \quad [\because x_1 x'_1 = 0]$$

$$\Rightarrow (x_1 x_3 + x_2 x'_1 x'_3)(x'_1 + x_2 + x'_3)$$

$$\Rightarrow x_1 x'_1 x_3 + x_1 x_2 x_3 + x_1 x_3 x'_3 + x_1 x_2 x'_3 x'_1 + x'_1 x_2 x_3 . x_2 + x'_1 x_2 x_3 x'_3 \quad [\because x_1 x'_1 = 0 \quad x_3 x'_3 = 0]$$

$$\Rightarrow x_1 x_2 x_3 + x'_1 x_2 x'_3 + x'_1 x_2 x'_3 + x'_1 x_2 x'_3 \quad [\because A.A = A]$$

$$\Rightarrow x_1 x_2 x_3 + x'_1 x_2 x'_3$$

* Question is wrong.

Q. 2. (d) (ii) Define

(1) Canonical form

(2) Standard form

(3) Sum of the products

(4) Product of the sums

(5) Don't care terms.

Ans. (1) Canonical form : The equation for the function can be formed either in SOP (Sum of product) or in POS (Product of Sum). These are also known as canonical forms.

(2) Standard form : There are two type of forms

(i) SOP (Sum of Product) $Y = \overline{A}B + A\overline{B}$

(ii) POS (Product of Sum) $Y = (\overline{A} + \overline{B}).(A + B)$

(3) Sum of product (SOP) Form: It is the sum of the implicants which provides the equation for the function in SOP form. For example,

$Y = \overline{A}B + A\overline{B}$

Here $\overline{A}B$ represent minterm (m_1) and $A\overline{B}$ represent minter (m_2)

So we can say, $Y = \Sigma m(1, 2)$

(4) Product of sums (POS) Form: It is the sum of compliments in input variables in each row is called maxterm.

For Example $Y = (A + B)(\overline{A} + \overline{B})$

Here term $(A + B)$ represent maxterm $= M_0$

and therm $(\overline{A} + \overline{B})$ represent maxterm $= M_3$

So we can say $Y = \Pi M(0, 3)$

(5) Don't care terms : A (d) means don't care i.e. it can be considered as 1 or 0.

Q. 2. (e) Explain, how do we measure the voltage, current and the phase of a wave form using the CRO ? 10

Ans. Voltage Measurement : Cathode Ray Oscilloscope (CRO) can be used for measurement of voltage of any electrical signal as the deflection of the electrostatic beam is directly proportional to the deflection plate voltages.

For measurement of direct voltage, firstly the spot is centered on the screen without applying any voltage signal to the deflection plates. Then, directly voltage to be measured is applied between a pair of deflection plates and deflection of the spot is observed on the screen. The magnitude of the deflection multiplied by the deflection factor gives the value of direct voltage applied.

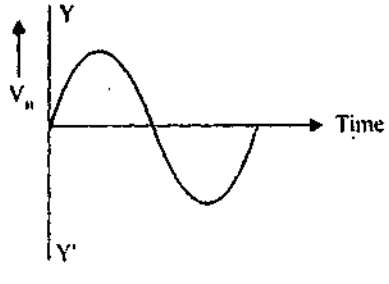
Usually, the screen is calibrated for fixed operating condition, so by reading the scale, voltage can be measured directly by CRO. The r.m.s value of a.c. voltage applied will be equal to this peak value divided by $2\sqrt{2}$ for sinusoidal wave form.

Current Measurement : For measurement of current, the current of under measurement is passed through a known non-inductive resistance and the voltage drop across it is measured by CRO, as mentioned above. The current can be determined simply by dividing the voltage drop measured by the value of non-inductive resistance. When the current to be measured is of very small magnitude, the voltage drop across non-inductive resistance (small value) is usually amplitude by a calibrated amplifier.

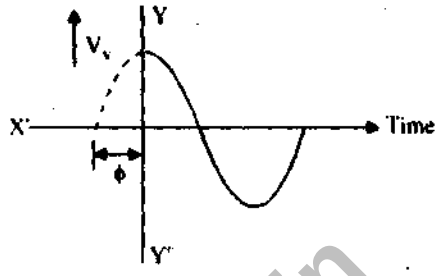
The current and voltage can be measured simultaneously by using double beam cathode ray oscilloscope.

Phase Measurement : We have discussed about the two sinusoidal voltage signals of equal frequency having some phase difference applied to the deflection plates of CRO, a straight line or an ellipse appears on the screen. In the case of straight line appearing on the screen, phase angle difference would be zero or 180° but in case of an ellipse, we will have to use a formula for determination of phase difference.

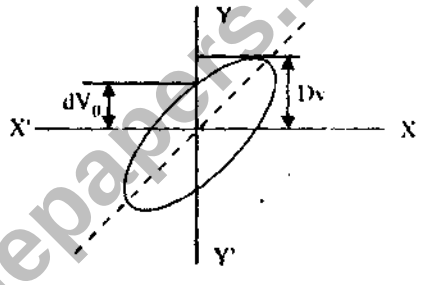
Let there be two sinusoidal voltage signals given by expressions



(a)



(b)



(c)

Fig.

$V_n = V_n \sin \omega t$

$V_v = V_v \sin(\omega t + \phi)$, where ϕ is the phase difference

Since, deflection is directly proportional to amplitude of voltage

$d_n = D_n \sin \omega t$

$d_v = D_v \sin(\omega t + \phi)$

$t = 0$, values of d_n and d_v are

$d_{n0} = 0$ and $d_{v0} = D_v \sin \phi$

So, $\sin \phi = \dfrac{d_{v0}}{D_v}$

Graphical meanings of d_{v0} and D_v are shown in figure. Thus, the phase difference between two sinusoidal voltages of equal frequency can be detarmined by measuring d_{v0} and D_v.

SECTION - C

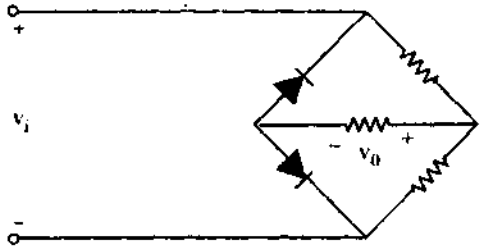
Note : *Attempt **all** questions.*

10 × 5 = 50

All questions carry equal marks.

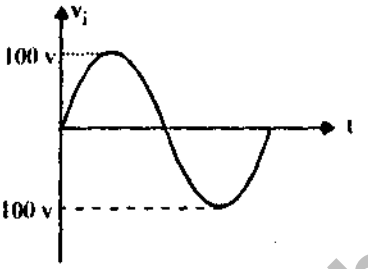
Q. 3. Attempt any two parts of the following :

(a) Sketch v_0 for the following circuit and determine the dc value of output voltage. Input to the circuit is 100 V peak to peak sine wave :

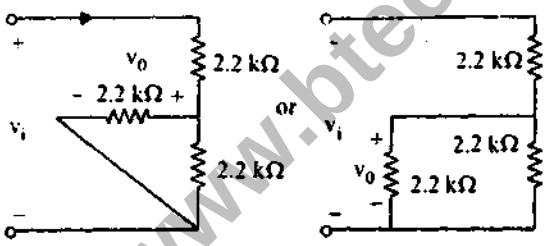


Diodes are ideal. All resistances are 2.2 kΩ

Ans. Given that



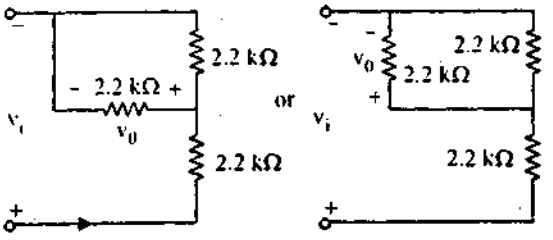
For (+ ive) half cycle



$$V_0 = V_i\left(\frac{1.1}{1.1+2.2}\right) \Rightarrow 100 \times \frac{1.1}{3.3} = \frac{100}{3}$$

= 33.3 Volt.

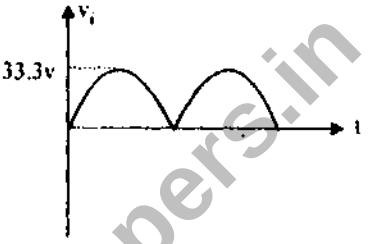
Similarly for (–ive) half cycle :



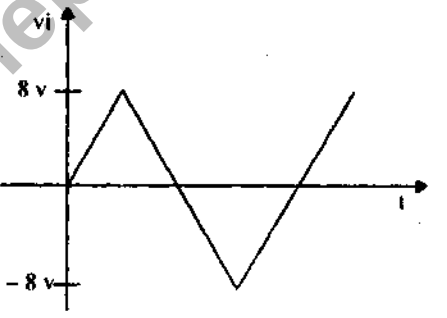
Again $V_0 = 100 \times \frac{1.1}{1.1+2.2}$

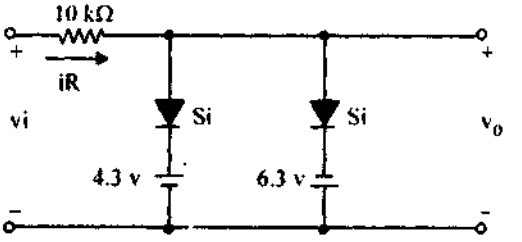
$V_0 = \frac{100}{3} = 3333$ Volt

Hence O/p waveform will be



Q. 3. (b) Sketch i_R and v_0 for the following circuit :

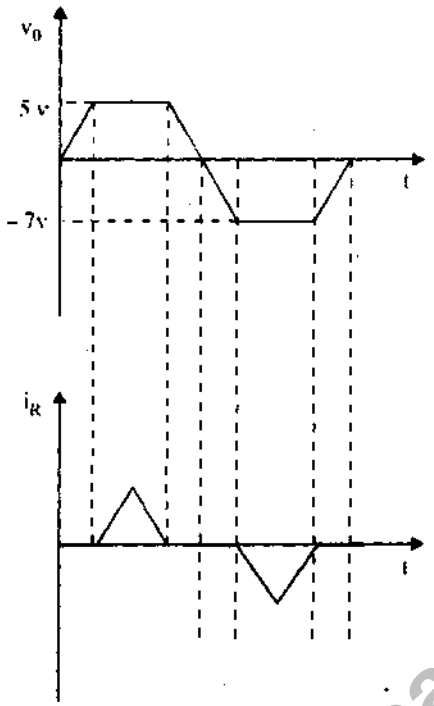




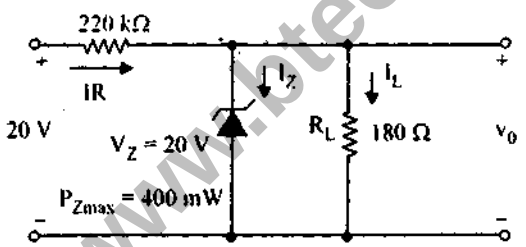
Ans. For + ive half cycle, before (5V) output voltage will be equal to input voltage, because 5V is required to conduct Si diode with 4.3 V battery.

Similarly for – ive the half cycle, 7V (6.3 + 0.7) is required to conduct Si diode with 6.3V battery.

Hence output waveform will be



Q. 3. (c) Determine V_L, I_L, I_Z and I_R for the following circuit.



Ans. $V' = 20 \times \dfrac{180}{220 + 180}$

$V' = 9$ V

Hence, Zener will be off because

$V_z > V'$

So the output voltage $V_L = V' = 9V$

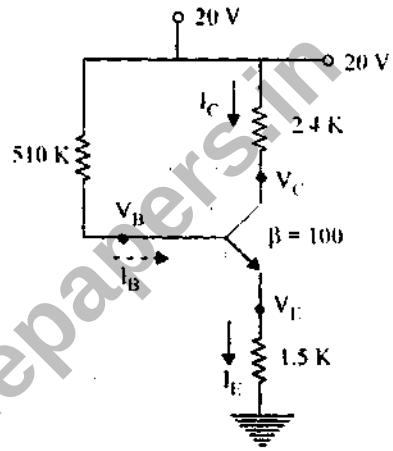
and $I_Z = 0$

$I_L = \dfrac{9}{180} = 0.05$ Amp

$I_R = I_L = 0.05$ Amp

Q. 4. Attempt any one of the following :

(a) Determine I_C, V_E, V_B, V_C and I_B for the following circuit.



Ans. Applying kVL,

$20 = 510\, I_B + 0.7 + 1.5\, I_E$

$20 - 0.7 = 510\, I_B + 1.5(I_B + I_C)$

$= 510\, I_B + 1.5(I_B + 100\, I_B)$

$= 661.5\, I_B$

$$I_B = \frac{19.3}{661.5} = 0.029 \text{ m Amp}$$

$I_c = 100 \times I_B = 100 \times 0.029 = 2.9$ m Amp

$V_E = I_E \times 1.5$

$= (2.9 + .029) \times 1.5$

$V_E = 4.39$ Volt

$V_{BE} = 0.7$

$V_B - V_E = 0.7$

$V_B = V_E + 0.7$

$V_B = 3.39 + 0.7$

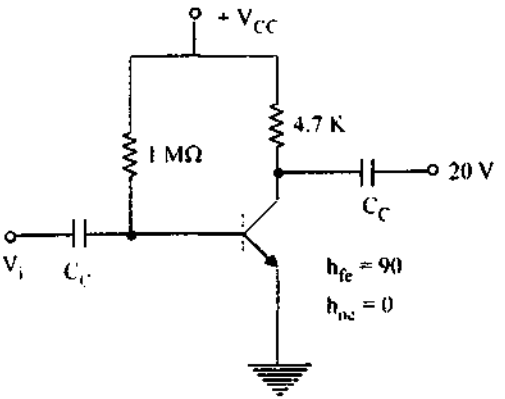
$V_B = 5.09$ Volt

$\because \quad 20 - V_C = 2.4\, I_C$

$V_C = 20 - 2.4 \times 2.9$

$V_C = 13.04$ Volt

Q. 4. (b) Determine V_{CC} for the following circuit if the voltage gain $A_V = -200$

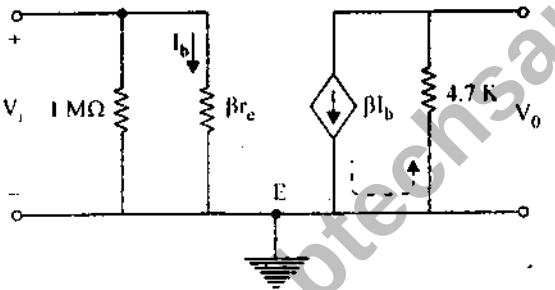


Ans. From. re Model

$$A_V = \frac{V_0}{V_i} = -\frac{\beta I_b \times (4.7\,k)}{\beta I_b\, r_e}$$

Given, $Av = -200$

$$-200 = -\frac{4.7 \times 10^3}{r_e}$$



$$r_e = \frac{4.7 \times 1000}{200}$$

$$r_e = 23.50\ \Omega$$

but, $r_e = \frac{26\text{ mV}}{I_{CQ}}$

$$I_{CQ} = \frac{26 \times 10^{-3}}{23.5} = 1.11\text{ mA}$$

Using DC Analysis

$V_{CC} = I_b \times 1 \times 10^6 + V_{BE}$

For Si Transistor $V_{BE} = 0.67$ V

$$V_{CC} = \frac{I_C}{\beta} \times 1 \times 10^6 + 0.7$$

[$\because \beta = h_{fe} = 90$]

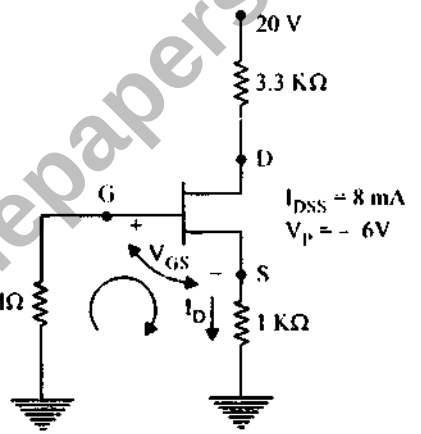
$$V_{CC} = \frac{1.11}{90} \times 10^{-3} \times 10^6 + 0.67$$

$$= 12.33 + 0.67$$

$$\boxed{V_{CC} = 13\text{ Volt}}$$

Q. 5. Attempt any one of the following :

(a) Determine V_{GS}, I_D, V_{DS} V_D, V_G and V_S for the following circuit:



Ans. $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$$I_D = 8\left(1 - \frac{V_{GS}}{-6}\right)^2 \quad \ldots(1)$$

$$-V_{GS} - I_D R_S = 0$$

$$V_{GS} = -I_D R_S$$

$$= -I_D \times 1$$

or $V_{GS} = -I_D$

Put the value of V_{GS} in equation (1)

$$I_D = 8\left[1 - \frac{(-I_D)}{-6}\right]^2$$

$$I_D = \frac{8}{36}[6 - I_D]^2$$

or $2I_D^2 - 33I_D + 72 = 0$

On solving $I_D = 13.91$ mA, 2.6 mA

Taking $\boxed{I_D = 2.6\text{ mA}}$

$\boxed{V_{GS} = -2.6\text{ Volt}}$

$\because V_{DD} - V_D = I_D R_D$

$20 - V_D = 2.6 \times 3.3$

$V_D = 11.42$ Volt

$\because V_S = I_D R_S = 2.6 \times 1$

$\boxed{V_S = 2.6 \text{ Volt}}$

$V_{DS} = V_D - V_S = 11.42 - 2.6$

$V_{DS} = 8.82$ Volt

$V_{GS} = V_G - V_S$

$V_G = V_{GS} + V_S$

$V_G = -2.6 + 2.6$

$\boxed{V_G = 0 \text{ Volt}}$

Q. 5. (b) (i) Enlist the characteristics of an ideal operational amplifier (op-amp). 3

(ii) Draw the circuit of a subtractor using op-amp and explain its working. 3

(iii) Determine the V_0 for the following circuit : 4

Ans. (i) For Ideal (Op-amp) :

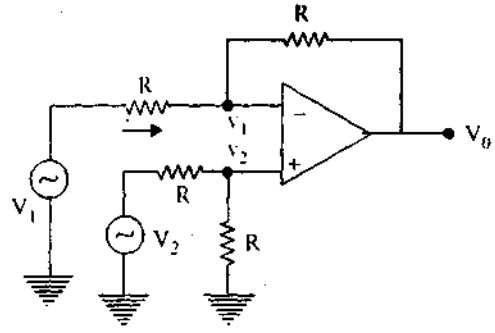
- Input impedance should be infinite.
- Output impedance should be zero.
- Voltage gain infinite.
- Infinite bandwidth
- Infinite CMRR.
- Infinite slew rate.

(ii) Subtructor

$\because v_1 = v_2 = V_2 \dfrac{R}{R+R} = \dfrac{V_2}{2}$

applying node at v_1,

$\dfrac{V_1 - v_1}{R} = \dfrac{v_1 - V_0}{R}$



$V_1 + v_0 = 2v_1$

$V_1 + v_0 = 2\dfrac{V_2}{2}$

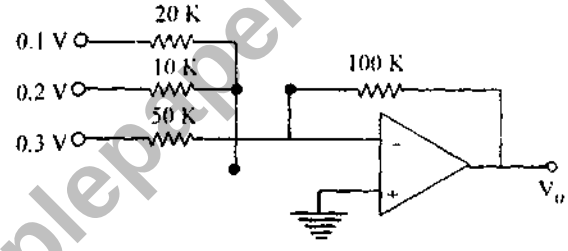
$\boxed{V_0 = V_2 - V_1}$

(iii)

$V_0 = -\left[\dfrac{100}{20}(0.1) + \dfrac{100}{10}(0.2) + \dfrac{100}{50}(0.3)\right]$

$\because V_0 = -\left(\dfrac{Rf}{R_1}V_1 + \dfrac{R_f}{R_2}V_2 + \dfrac{R_f}{R_3}V_3\right)$

$\boxed{V_0 = -3.1 \text{ Volt}}$



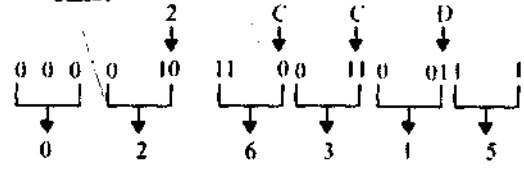
Q. 6. Attempt any two of the following :

Q. 6. (a) Convert the following numbers :

$(2CCD)_{16} = (\quad)_8 = (\quad)_5$

$(7841)_9 = (\quad)_{10} = (\quad)_4 = (\quad)_2$

Ans.



$\Longrightarrow (0\,2\,6\,3\,1\,5)_8$

Now

$2 \times 16^3 + 12 \times 16^2 + 12 \times 16^1 + 13 \times 16^0$

$= 11469$

5	11469	
5	2293	4
5	458	3
5	91	3
5	18	1
5	3	3

$(3\,3\,1\,3\,3\,4)_5$

$(7841)_9 = (\quad)_{10}$

$= (\quad)_4 = (\quad)_2$

$7 \times 9^3 + 8 \times 9^2 + 4 \times 9^1 + 1 \times 9^0$

$= (5788)_{10}$

2	5788	
2	2894	0
2	1447	0
2	723	1
2	361	1
2	180	1
2	90	0
2	45	0
2	22	1
2	11	1
2	5	1
2	2	2
	1	0

$(1011110011100)_2$

4	5788	
4	1447	0
4	361	3
4	90	1
4	22	2
4	5	2
	1	1

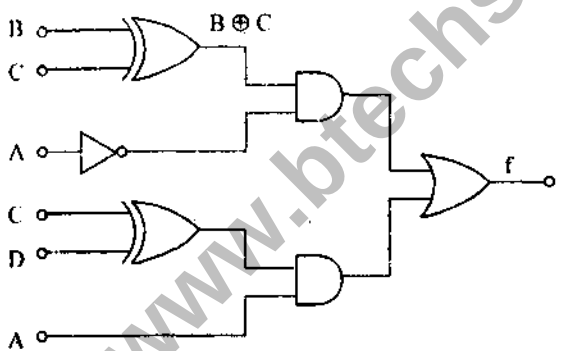
$(1122130)_4$

Q. 6. (b) Realize the following expression using Ex-OR/Ex-NOR gates and basic gates if required.

$$f(A, B, C, D) = A'BC' + A'B'C + AC'D + ACD'$$

Ans. $= A'(BC' + B'C) + A(C'D + CD')$

$= A'(B \oplus C) + A(C \oplus D)$



Q. 6. (c) Minimize the given functlon using K-map and convert the minimized function into POS form

$f(A, B, C, D) = \Sigma\, m(1, 3, 5, 7, 9, 10, 12, 13)$

Ans.

$f(A, B, C, D) = \Sigma\, m(1, 3, 5, 7, 9, 10, 12, 13)$

For SOP Form

$f = \overline{C}D + \overline{A}D + AB\overline{C} + A\overline{B}C\overline{D}$

Now taking,

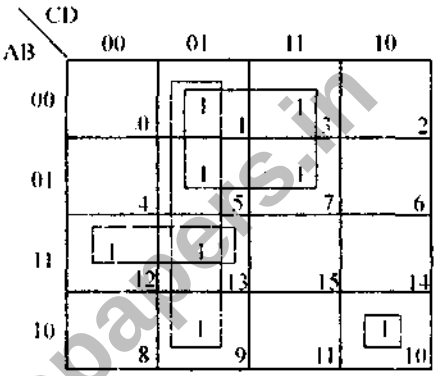
$\bar{f} = \overline{\overline{C}D + \overline{A}D + AB\overline{C} + A\overline{B}C\overline{D}}$

for POS Form $\Rightarrow$

$(\overline{\overline{C}D})(\overline{\overline{A}D})(\overline{AB\overline{C}})(\overline{A\overline{B}C\overline{D}})$

$\bar{f} \Rightarrow (C + \overline{D}).(A + \overline{D})$

$.(\overline{A} + \overline{B} + C)(\overline{A} + B + \overline{C} + D)$



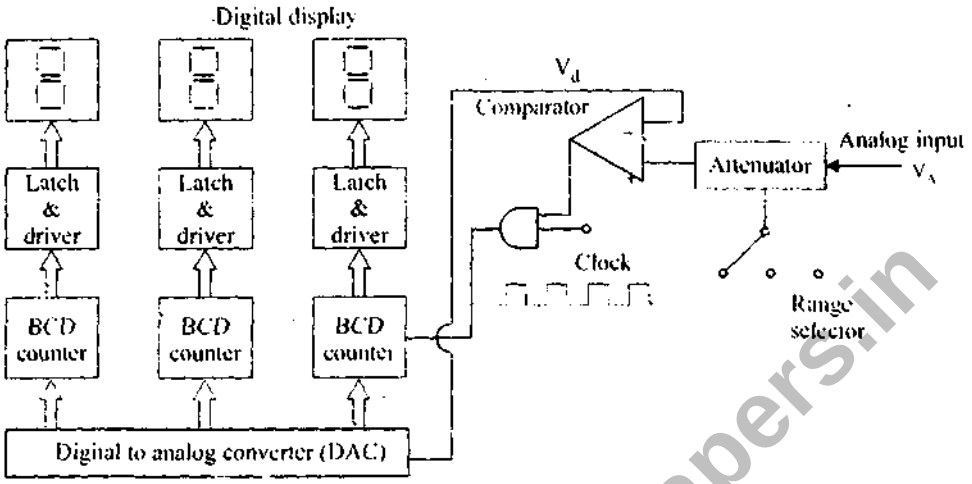
Q. 7. Attempt any one part of the following.

Q. 7. (a) Explain the working of digital voltmeter with help of a block diagram.

Ans. Digital Voltmeter (DVM) : A digital voltmeter displays the value of a.c or d.c. voltage being measured directly as discrete numerals, in the decimals number system. DVM eliminates the overvational errors committed by operators. The error on account of approximations are entirely eliminated. The use of DVM increases the speed of operation. The output of digital voltmeter can be fed to memory devices for storage and future application.

(1) Operation : The analog input voltage V_A is applied to the noninverting terminal of a comparator through the attenuator The inverting terminal is connected to the output of digital to analog converter. Initially the output of digital to analog (DAC) converter is zero. Therefore $V_A > V_d$ and the comparator output will be high. This will enable the AND gate and clock pulses, which are passed through the chain of BCD counters. The counter are initially reset. As soon as clock pulses are applied to them, they start counting.

As counter output increases the DAC output V_d will be also increases. As long as



$V_A > V_d$ the AND gate remains enabled and counting continues to take place.

But as $V_A < V_d$

Q. 7. (b) Explain the working of CRO with the help of a block diagram.

Ans. The cathode Ray Oscilloscope (CRO) is an extremely useful and variable laboratory instrument used for studying wave shapes of alternating currents and voltages as well as for measurement of voltages, current, power and frequency, in fact, almost any quantity that involves amplitude and waveform. It allows the user to see the amplitude of electrical signals as a function of time on the screen. It is widely used for troubleshooting radio and TV receivers as well as laboratory work involving research and design. It can also be employed for studying the wave shaped of a signal with respect to amplitude distortion and deviation from the normal. In true sense, the Cathode Ray Oscilloscope (CRO) has been one of the most important tools in the design and development of modern electronic circuit.

Block Diagram : The instrument employs a cathode ray tube, which is the heart of the oscilloscope. It generates the electron beam, accelerates the beam to a high velocity, deflects the beam to create the image and contains a phosphor screen whose the electron beam eventually becomes visible.

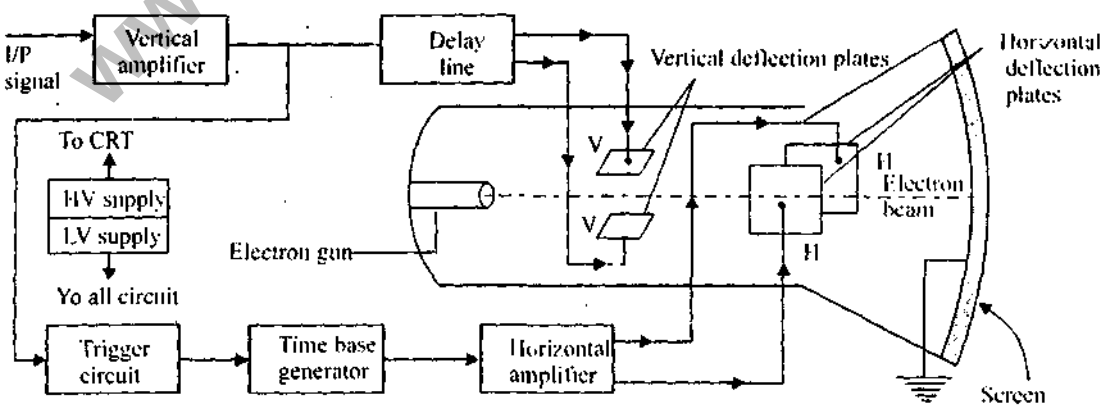


Fig. Block diagram of CRO