B.Tech.

FIRST SEMESTER EXAMINATION, 2010-11

ELECTRONICS ENGINEERING

(EEC-1011)

Time : 3 Hours] *[Total Marks : **100***

Note : *(1) Attempt **all** questions. All questions carry equal marks. Assume any data, not given, suitably.*

SECTION-A

Q. 1. Attempt all the parts of this question. All parts of the question carry equal marks. These questions contain 10 objectives/fill in the blank type/true-false type questions. $2 \times 10 = 20$

(i) The knee voltage of a p-n junction is ..... after doping.

Ans. 0.3 for Germanium and 0.7 for silicon.

(ii) The Zener diode work as

(a) Current regulator **(b) Voltage regulator**

(c) Power regulator **(d) Both (a) and (b)**

Ans. (b) The Zener diode works as voltage regulator.

(iii) PIV of all the diodes of center-Tapped-transformer-full-wave- rectifier is .....

Ans. PIV of all the diodes of center-Tapped-Transformer-full-wave rectifier $2V_m$.

(iv) The biasing circuit which gives best stability to the Q point is

(a) Base resistor biasing **(b) Emitter resistor biasing**

(c) Potential divider biasing **(d) Feed back resistor biasing**

Ans. The biasing circuit which gives best stability to the *Q*-Point is Potential divider biasing.

(v) The parameters α and β of a bipolar junction transistor is related as .....

Ans. The parameter α and β of bipolar function Transistor is related as

$$\beta = \frac{\alpha}{1 - \alpha}$$

(vi) The gate of a depletion type MOSFET is made up of

(a) metal **(b) semiconductor**

(c) both **(d) none**

Ans. (a) The Gate of a depletion type MOSFET is made up metal.

(vii) The input impedance of a JFET is

(a) Very high **(b) Very low**

(c) Moderately high **(d) Moderately low**

Ans. (a) The input impedance of JFET is very high.

(viii) The De Morgan's Theorem states that ..... .

Ans. The De Morgan's theorem states that "complement of sum of variable is equal to product complement of individual variable."

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

"The complement of product of variable is equal to sum of individual complement of individual.

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

(ix) The CRO can measure

(a) phase **(b) voltage**

(c) current **(d) none of these**

Ans. The CRO can measure (a) Phase (b) Voltage (c) Current

(x) The full-scale deflection of ohm scale in a multimeter reads

(a) Infinity resistance **(b) Zero resistance**

(c) Some finite resistance **(d) none of tbe above.**

Ans. The full scale deflection of ohm in multimeter reads.

SECTION-B

Q. 2. Attempt any tbree parts of the following : **10 × 3 = 30**

(a) Define and explain the following terms in respect of p-n junction.

(i) depletion layer. (ii) barrier potential, (iii) AC and DC resistance, (iv) Diffusion and transition capacitance. (v) PIV, (vi) ripple factor.

Ans. Depletion Layer: When a free electron meets a free holes, it makes electron hole natural pair. So for as charge movements are concerned this means the holes and electron cancel each other and vanish. Thus at boundary, there is an area that does not have any mobile charge barrier. This is called depletion region or depletion layer.

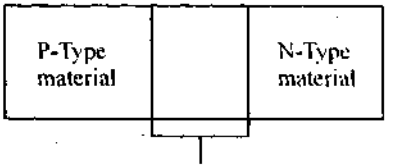


Fig. (a)

(ii) Potential barrier: The neutral area provide the barrier for the further movement of the charge carriers that's why it is called potential barrier. See the figure (a).

(iii) DC Resistance: The Resistance of the diode at certain operating point can be found by finding the corresponding potential difference across the diode V_D and the current through diode I_D. Thus the *DC* resistance is

$$R_D = \frac{V_D}{I_D}$$

AC Resistance: The changes in the voltage and current can be used to determine the ac resistance for a certain region of the diode characteristics the ac resistance can be written as

$$r_{ac} = \frac{\Delta V_D}{\Delta I_D}$$

(iv) Transition Capacitance: As the depletion region near the p–n junction contains immobile positive charges on n region and immobile negative charges on p region, which creates parallel plate capacitor, the P and N Type region on either side having low resistance act as plate while the depletion region act as dielectric material this junction capacitance is called as space charge or transition capacitance and represented by C_T

$$C_T = \frac{\varepsilon A}{d}$$

Where A = Cross sectional area of the junction.

So, C_T is variable capacitance which decreases when applied voltage increases, as the depletion width decreases with increase in forward bias.

(v) Diffusion capacitance: This occurs in forward bias, due to injected charge stored on the both side of the junction outside the space charge region. It is represented by C_D and defined as the rate of change of injected charges with applied voltage

$$C_D = \frac{dQ}{dV} = \frac{CeI}{\eta KT}$$

$$C_D >> C_T$$

(vi) Ripple Factor : The ripple factor is defined as the ratio of the effective value of the A.C. components of voltage or current present in the output from the rectifier to the direct or average value of the output voltage or current.

Ripper factor, $r = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I^2 - I_{dc}^2}}{I_{dc}}$

$\Rightarrow$ $r = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$

$\Rightarrow$ $r = \sqrt{K_f^2 - 1}$

where, K_f is the form factor of the input voltage. For half wave rectifier, the form factor is given as,

$$K_f = \frac{I_{r.m.s}}{I_{a.v}} = \frac{I_{max/2}}{i_{max/\pi}} = \frac{\pi}{2} = 1.57$$

so, Ripple factor, $r = \sqrt{(1.57)^2 - 1} = 1.21$

Q. 2. (b) Explain the h-parameter model of a Bipolar junction Transistor.

Ans. Small Signal Model Using h-Parameters : Another way of finding the A.C. model is with the help of characteristics of a transistor in the case of CE configuration.

From the input characteristics it is clear that input voltage V_{BE} is the function of input current I_B and the output voltage V_{CE}, *i.e.*,

$$V_{BE} = f(I_B, V_{CE}) \qquad ...(1)$$

For A.C. analysis, only time changes are important some may write

$$\frac{\partial V_{BE}}{\partial t} = \frac{\partial V_{BE}}{\partial I_B} \times \frac{\partial I_B}{\partial t} + \frac{\partial V_{BE}}{\partial V_{CE}} \times \frac{\partial V_{CE}}{\partial t} \qquad ...(2)$$

$$\frac{\partial V_{BE}}{\partial t} = h_{ie}\frac{\partial I_B}{\partial t} + h_{re}\frac{\partial V_{CE}}{\partial t} \quad ...(3)$$

As only the time derivative in values shows the A.C. components (if we are studying sinusidual A.C. signal) then

Time derivative of sinusidual signal = Sinusidual signal

$$V_{BE} = h_{ie}I_B + h_{re}V_{CE} \quad ...(4)$$

From the output characteristics it is clear that output current I_C is the function of current I_B and output voltage V_{CE}.

So, $$I_C = f(I_B, V_{CE}) \quad ...(5)$$

Again $$\frac{\partial I_C}{\partial t} = \frac{\partial I_C}{\partial I_B} \times \frac{\partial I_B}{\partial t} + \frac{\partial I_B}{\partial V_{CE}} \times \frac{\partial V_{CE}}{\partial t} \quad ...(6)$$

Again for applied A.C. signal

$$I_C = h_{fe}I_B + h_{oe}V_{CE} \quad ...(7)$$

So, we can represents the transistor in two equations

$$V_{BE} = h_{ie}I_B + h_{re}V_{CE} \quad ...[Eqn.(4)]$$

$$I_C = h_{fe}I_B + h_{oe}V_{CE} \quad ...[Eqn.(7)]$$

where $$h_{ie} = \left.\frac{\partial V_{BE}}{\partial I_B}\right|_{\text{at } V_{CE}=0} \quad ...(8)$$

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{\text{at } V_{CE}=0} \quad ...(9)$$

That shows the *input impedance of transistor when output is short circuit.*

$$h_{re} = \left.\frac{\partial V_{BE}}{\partial V_{CE}}\right|_{\text{at } I_B=0} \quad ....(10)$$

$$= \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{\text{at } I_B=0} \quad ...(11)$$

That shows the *reverse voltage gain when input is open circuit.*

$$h_{fe} = \left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}=0} \quad ...(12)$$

$$h_{re} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=0} \quad ...(13)$$

This shows *forward current gain when output is short circuit*

$$h_{oe} = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{I_B=0} \quad ...(14)$$

$$= \frac{\Delta I_C}{\Delta V_{CE}} \cdot \quad ...(15)$$

At shows the *output admittance when input open circuit.*

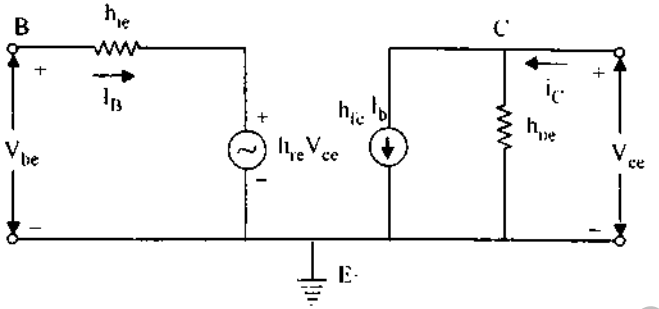


Fig. h-Parameter model for CE configuration.

(Suffix e, h_{ie}, h_{re}, h_{oe} h_{fe} shows that we are studying the common emitter configuration. Final model has been drawn in Figure.

This representation is called hybrid parameter representation.

Q. 2. (c) Explain the working of p-channel JFET. Draw the I_D vs V_{DS} of the following circuit.

Ans. P-type JFET: The only difference between P-type and N-type JFET is that P regions are replaced by N-type and N regions are replaced by P-type, Due to this replacement, the polarities of voltages are changed.

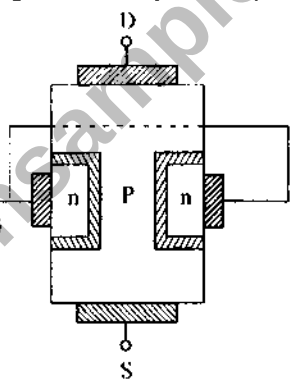


Fig. P-JFET

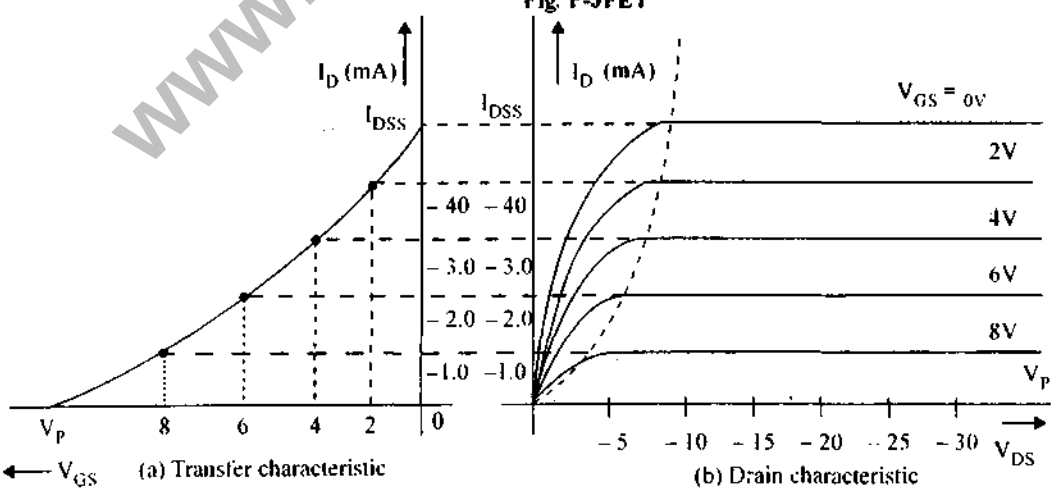


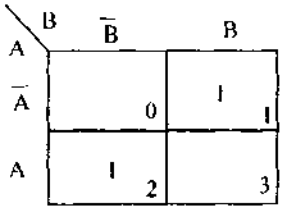
Fig. Characteristics of P-JFET.

Q. 2. (d) Draw and explain the binary half-adder and half-subtractor circuits. How tbey are used to work as full adder and full subtractor circuits.

Ans. Half adder :

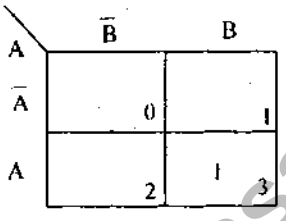
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

for Sum :



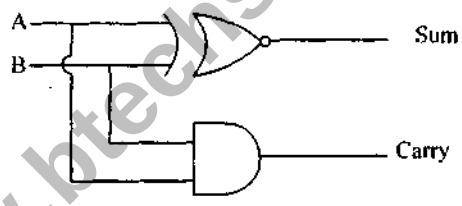
$S = \overline{A}B + A\overline{B} = A \oplus B$

for carry



$C = AB$

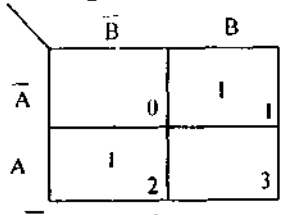
Circuits :



Half Suhtractors :

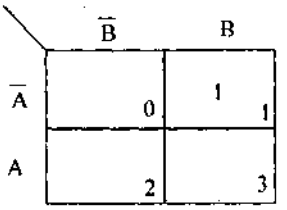
A	B	Sub	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Sub :

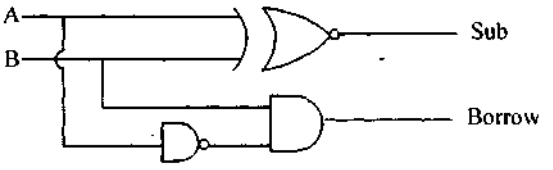


Sub = $A\overline{B} + \overline{A}B = A \oplus B$

Borrow



$B = \overline{A}B$

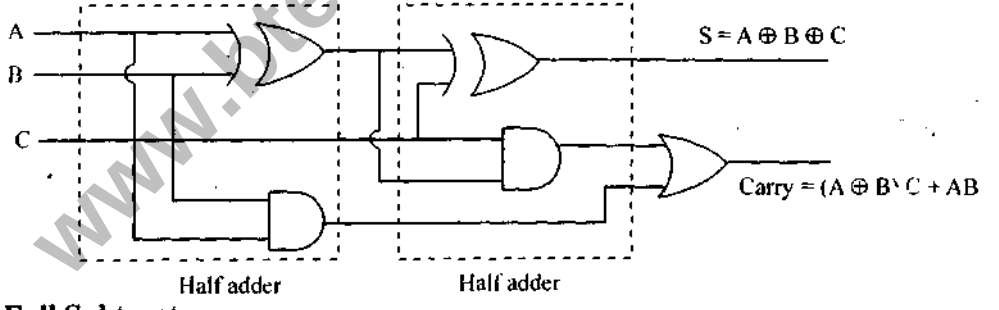


Full adder :

A	B	C	Sum (S)	Carry (C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC = A \oplus B \oplus C$

$C = \overline{A} + BC + A\overline{B}C + AB\overline{C} + ABC = AB + AC + BC$



Full Subtractor :

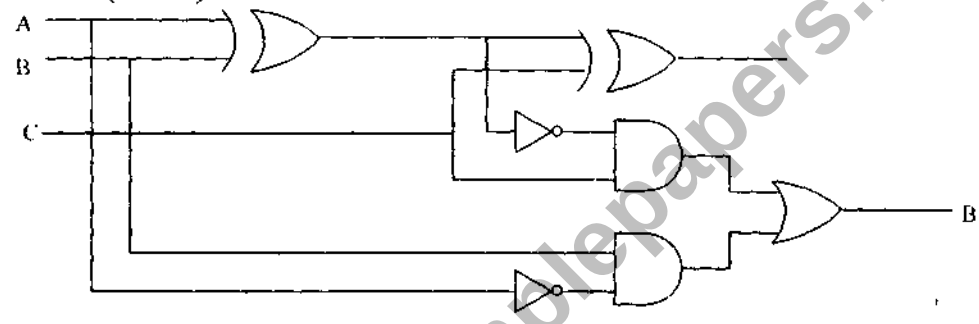
A	B	C	Sub	Borrow B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1

1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Borrow :

$$= \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + ABC = \overline{(A \oplus B)}C + \overline{A}B$$

$$\text{Sub} = C\overline{(A \oplus B)} + \overline{C}(A \oplus B) = A \oplus B \oplus C$$



Q. 2. (e) With the help of block diagram explain the working of digital multimeter. What are the characteristics of Digital Voltmeter used in a typical digital multimeter?

Ans. Digital Multimeter: Digital multimeter is a device that can measure voltage, current, resistance etc. That's why it is a compulsory part of every electrical and electronic engineer. The simplified block diagram has been drawn here.

The block diagram has the following parts.

1. *Range switches* : The input voltage, current or ohm signals are conditioned by the function and selector switches to produce the output with in range.
2. *External oscillator* : Timing for the overall operation of the A/D converter is derived from an external oscillator whose frequency is selected to be 40 kHz.
3. Current shunt : If current is to be read, it is converted to a DC voltage via internal shunt resistors.
4. A/D (analog to digital) converter : Here the DC voltage amplitude is changed into a digital format. The resulting signals are processed in the decoders to light the appropriate LCD segments.
5. *Internal voltage source* : For resistance measurements, an internal voltage source supplies the necessary voltage.
6. *Voltage divider* : With the help of voltage divider, the high input voltage is limited to the range of the meter.
7. Display : Digitized measurements data is presented to the display as four decoded digits (seven segments) plus polarity. Decimal point position on the display is determined by the selector switch setting.

In all measurement we measure voltage and display it in display device. When input is convert into pulse and count by counter. That will be in form of voltage.

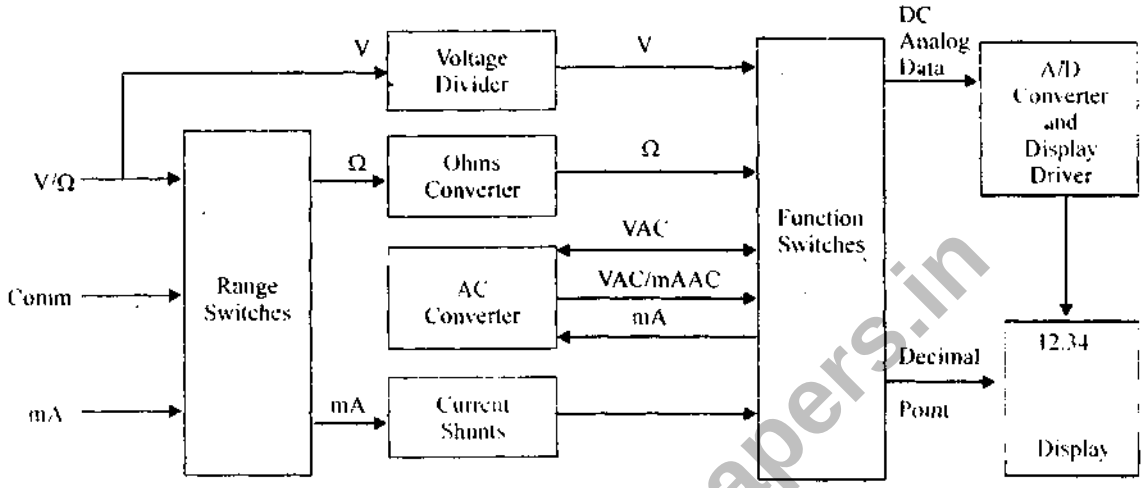


Fig. Block diagram of digital multimeter (DMM)

SECTION-C

Note: Attempt all the questions. All questions carry equal marks. **(10× 5 = 50)**

Q. 3. Attempt any two parts of the following : **5 × 2 = 10**

(a) Show that the maximum efficiency of Half wave rectifier is 40.6%.

Ans. The efficiency of Half wave Rectifier is Ratio of output dc power to input AC power.

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = \frac{v^2_{dc}}{R} = \frac{(V_m/\pi)^2}{R_L}, \quad P_{ac} = \frac{V_{ac}^2}{R} = \frac{(V_m/2)^2}{R_L + R_f}$$

then $$\frac{V_m^2(R_L + R_f)}{R_L(V_m^2/4)} = \frac{4}{\pi^2}\left[\frac{R_L + r_f}{R_L}\right] = \frac{4}{\pi^2}\left[1 + \frac{r_f}{R_L}\right]$$

for Ideal diode $r_f = 0$

$$\eta = \frac{4}{\pi^2}$$

$$\eta = 0.406 \boxed{= 40.6\%}$$

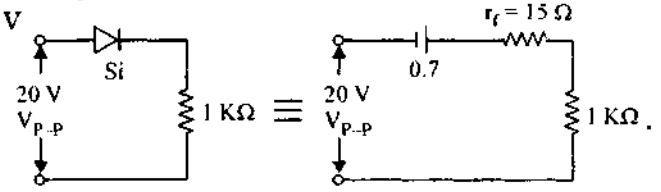
Q. 3. (b) An ac voltage of peak value 20V is connected in series with a Si diode and load resistance of 1 KΩ. If the forward resistance of diode is 15Ω. Find(i) peak current through diode (ii) Peak output voltage.

Ans. $V_{P-P} = 20$ V

peak current through diode

$$20 - I_{f_{p-p}}(15 + 1000) = 0$$

$$I_{f_{p-p}} = \frac{20}{1050} = 0.0197 = 19.7 \text{ mA}$$



Peak o/p voltage $V_{out(p-p)} = 1 \times 10^3 \times 19.7 \times 10^{-3}$

$$V_{out(p-p)} = 19.7 \text{ V}$$

Q. 3. (c) Describe the working of clamping circuit with neat diagrammes.

Ans. Clamper Circuits: Clamper Circuits, or briefly clampers are used to change the D.C. level of a signal to a desired value (Figure)

Clamping circuit uses a capacitor and a diode connection. When diode is in its on state, the output voltage equals to diode drop voltage (ideally zero) plus the voltage source, if any. Now let us examine the clamping process for the circuit in Figure.

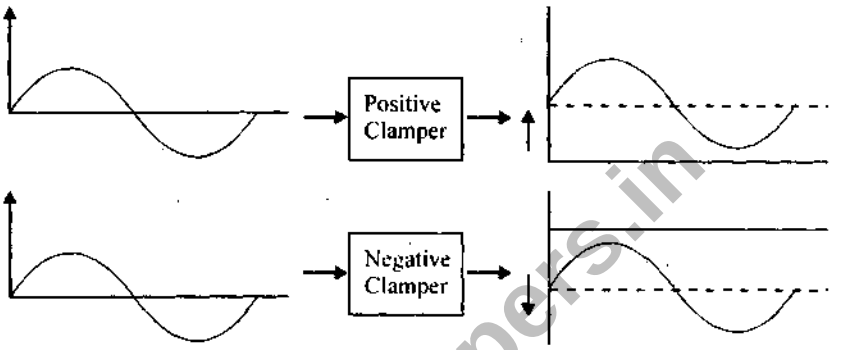


Fig. Clamper circuit.

As you know, this circuit, in fact, is a series R–C circuit. The resistance of diode (several ohms above its drop voltage) and the small capacitance yield to a small time-constant for this circuit. This means that the capacitor will rapidly be charged if any input voltage, that is enough to switch on the diode, is applied. The diode will conduct during the positive cycle of the input signal (Figure) and output voltage will be ideally zero (in practice this voltage equals ~ 0.6 V).

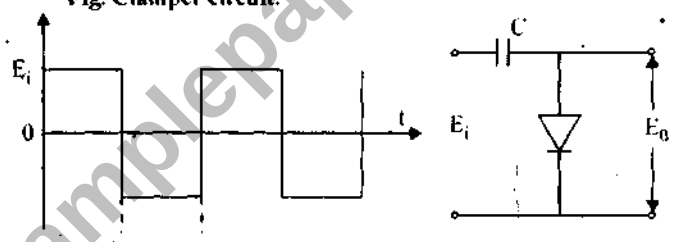


Fig. Typical clamping circuit.

Q. 4. Attempt any one part of the following : $10 \times 1 = 10$

(a) (i) Ir a CE transistor amplifier circuit, V_{CE} is increased from 2 to 12 V, the collector current changes from 3 to 4 mA, determine the output resistance.

Ans. In CE configuration change in o/p voltage $\Delta V_{CE} = 12 - 2 = 10$ V

Change in o/p current $\Delta IC = 4 - 3 = 1$ mA

o/p Resistance $= \dfrac{\Delta V_{CE}}{\Delta IC} = \dfrac{10}{1\text{ mA}} = 1\text{ k}\Omega$

Q. 4. (a) (ii) In a n-p-n transistor $\alpha = 0.98$, $I_E = 10$ mA, leakage current $I_{CBO} = 1\ \mu$A. Determine I_C I_B, β, I_{CEO}.

Ans. (ii) In n-p-n Transistor

$$\alpha = 0.98,\ I_E = 10\text{ mA},\ I_{CBO} = 1\ \mu\text{A}$$

$$I_C = \alpha I_E + I_{CBO} = 0.98 \times 10 \times 10^{-3} + 1 \times 10^{-6} = 9.8 \times 10^{-3} + 0.001 \times 10^{-3} = 9.801\text{ mA}$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \frac{0.98}{0.02} = 49$$

$$I_C = \beta I_B \Rightarrow \qquad I_B = \frac{I_C}{\beta} = \frac{9.801 \times 10^{-3}}{49} = 0.20002 \times 10^{-3} = 200\ \mu\text{A}$$

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = \frac{1\times 10^{-6}}{1-0.98} = \frac{10^{-6}\times 100}{0.02}$$

$$\boxed{I_{CEO} = 50\,\mu A}$$

Q. 4. (b) Why biasing is needed in a BJT ? Whicb of tbe biasing circuit is most preferred and why ? Explain in detail.

Ans. Biasing is needed in BJT for make stable the operating point or Q-point or to operate the BJT in a particular. Region like active Region, cut-off Region and saturation Region.

Potential divider biasing is most preferred because it is most stable biasing in BJT

Potential divider biasing : Self Bais :

It is also called voltage divider or potential divider.

Circuit Analysis. Figure

(*i*) Connect a voltage divider circuit across power supply and ground output of this is fed to base of transistor. So it is called voltage divider or potential divider biasing.

(*ii*) Due to the lower resistance of voltage divider the transistor is forward biased.

(*iii*) Now we see that power supply V_{CC} is connected to output directly that will cause to flow collector current even if no base current it also make possible to less dependence of collector current upon base current.

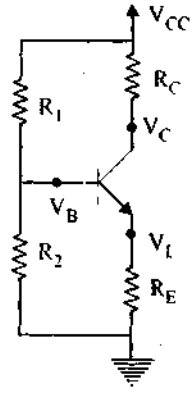


Fig. (a) Self biased.

Mathematical Analysis

(*i*) Solve voltage divider circuit by Thevenin theorem. Find a value of voltage with a series resistance that will be connected to the base of transistor.

(*ii*) Take a point at base-emitter junction.

(*iii*) Search a path towards ground connected to emitter from the point.

(*iv*) Search a path supply from the point. Be careful this path should be inside the transistor because we don't have information about V_{BC}.

Advantage

(*i*) Very good stability so very much used.

Mathematical Analysis

There we will see that due to supply V_{CC}, voltage V_B is generated at base of transistor. So, it is called self biased (It don't need any external input for I_B).

Now separate voltage divider circuit.

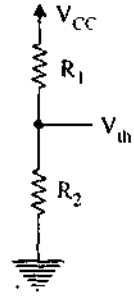


Fig. (b) Thevenin voltage.

So
$$\boxed{V_{Th} = \frac{R_2}{R_1 + R_2}.V_{CC}} \quad ...(1)$$

shows the value of voltage due to this voltage divider circuit.

Now to calculate equivalent resistance, ground the supply V_{CC}.

Then
$$\boxed{R_{Th} = R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2}} \quad ...(2)$$

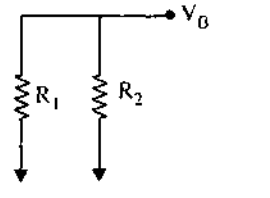


Fig. (c) Thevenin resistance

This analysis shows that base circuit (voltage divider) can be replaced by a equivalent voltage in series with a equivalent resistance. This is known as Thevenin theorem of network.

So, Thevenin's equivalent circuit can be drawn as in Figure.

(*i*) Applying KVL law

$$V_{Th} - V_{BE} = I_B(R_{Th}) + I_E R_E \quad ...(3)$$

$$V_{Th} - V_{BE} = R_{Th} I_B + I_E R_E$$

But $I_E = (1 + \beta) I_B$

$$V_{Th} - V_{BE} = R_{Th} I_B + (1 + \beta) I_B R_B$$

$$\boxed{I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_B}} \quad ...(4)$$

(*ii*) Now $I_{CQ} = \beta I_B + (1 + \beta) I_{CBO} = \beta I_B$ (Neglecting I_{CBO})

$$\boxed{I_{CQ} = \beta \cdot \frac{(V_{Th} - V_{BE})}{R_{Th} + (1 + \beta) R_B}} \quad ...(5)$$

(*iii*) $V_{CEQ} = V_C - V_E$

$$\boxed{V_{CEQ} = V_{CC} - I_C R_C - I_E R_E} \quad ...(6)$$

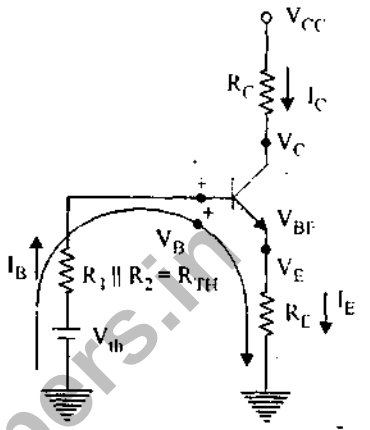


Fig. Solved circuit.

Q. 5. Attempt any one part of the following : **10 × 1 = 10**

(a) Explain the characteristics of an ideal operational amplifier. Sketch unity gain amplifier and non-inverting amplifier and find the output voltages in terms of input voltage. Explain why the operational amplifier is called operational amplifier?

Ans. Ideal OP-AMP : Several assumptions have to be made before the ideal op-amp analysis can proceed. These assumptions are also called the characteristics of ideal op-amp. These are as given below.

1. The **current flow into the input leads of the ideal op-amp is zero** when no external source is applied. This is called offset current which is not due to any external sources.

2. Second, **the ideal op-amp gain is assumed to be infinite,** hence it drives the output voltage to any value to satisfy the input conditions. This assumes that the op-amp output voltage can achieve any value. In reality, saturation occurs when the output voltage comes close to a power supply.

3. **The output voltage of ideal op-amp is zero until the voltage between the input leads is zero.**

4. The voltage between the input leads is zero when no external voltage is applied. It also means that if one input is tied to a hard voltage source such as ground, then the other input is at the same potential. The current flow into the input leads is zero, so **the input impedance of the op-amp is infinite.**

5. **The output impedance of the ideal op-amp is zero.** The ideal op-amp can drive any load without an output impedance dropping voltage across it. The output impedance of most op-amps is a fraction of an ohm for low current flows, so this assumption is valid in most cases.

6. **The frequency response of the ideal op-amp is flat;** this means that the gain does not

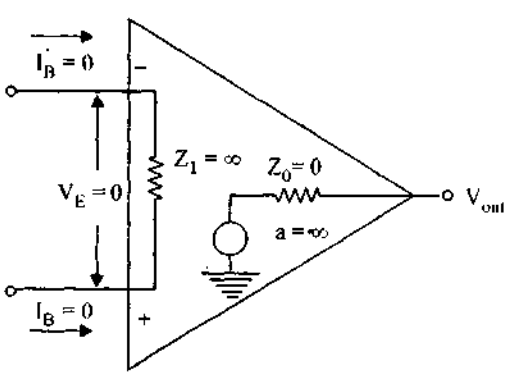


Fig. Ideal op-amp equivalent circuit.

vary as frequency increases. By constraining the use of the op-amp to the low frequencies, we make the frequency response ssumption true.

7. Ideal op-amp **only amplifies the difference of the applied signal.**

The Noninverting Op-amp :The noninverting op-amp has the input signal connected to its noninverting input (Figure) thus its input source sees infinite impedance. Hence the negative input must be at the same voltage as the positive input. The op-amp output drives current into R_F until the negative input is at the voltage, V_{IN}. This action causes V_{IN} to appear across R_G.

The voltage divider rule is used to calculate V_{IN}; V_{OUT} in the input to the voltage divider and V_{IN} is the output of the voltage divider. Since no current can flow into either op-amp lead, use of the voltage divider rule is allowed. Equation is written with the aid of the voltage divider rule, and algebraic manipulation yields equation in the form of a gain parameter.

$$V_{IN} = V_{OUT} \frac{R_G}{R_G + R_F} \qquad ...(1)$$

$$\boxed{A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_G + R_F}{R_G} = 1 + \frac{R_F}{R_G}} \qquad ...(2)$$

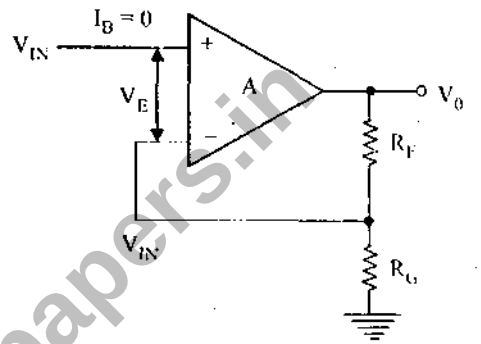


Fig. Noninverting Op-amp.

Unity gain configuration/voltage followers

When R_G becomes very large with respect to R_F.

$$(R_F / R_G) \approx 0 \qquad ...(3)$$

and Equation reduces to Equation

$$V_{OUT} = 1 \qquad ...(4)$$

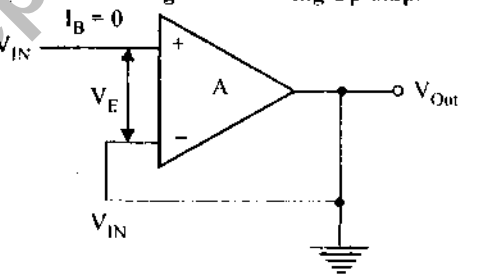


Fig. Unity gain configuration.

Under these conditions $V_{OUT} = 1$ and the circuit becomes a unity gain buffer. R_G is usually deleted to achieve the same results, and when R_G is deleted, R_F can also be deleted (R_F must be shorted when it is deleted). When R_F and R_G are deleted, the op-amp output is connected to its inverting input with a wire.

Q. 5. (b) Explain pinch off voltage, maximum saturation source current and trans conductance of a FET. A FET has tbe trans conductance of 3500×10^6 mbo and the load resistance is 10 kΩ and is used in voltage amplifier circuit. Calculate tbe voltage amplification assuming that $r_d >> R_L$.

Ans. The trans conductance (g_m) is a parameter for the measurement of the gain of FET. Through gm varies with the variation in the V_{GS}, we are interested in the value of gm in the pinch-off region.

It is given as :

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{constant}} \qquad ...(1)$$

or
$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \qquad ...(2)$$

where,
$$g_{mo} = \frac{-2I_{DSS}}{V_P} \qquad ...(3)$$

These are only the alternative representation of equation. In data sheet it is represented by Y_{of},

$$g_m = Y_{of} \quad ...(4)$$

Q. 6. Attempt any two parts of the following : **5 × 2 = 10**

(a) Whether the following expressions are true or false? State the theorems used.

(i) $AB + ABC + A'B + AB'C = B + AC$ **(ii)** $AB + AC + BC' = AC + BC'$

Ans. L.H.S.

$$= AB + ABC + A'B + AB'C = AB + B(AC + A') + AB'C$$
$$= AB + B(A + A')(A' + C) + A - B'C = AB + A'B + BC + AB'C$$
$$= B(A + A') + C(B + B'A) = B + C(B + B')(B + A)$$
$$= B + BC + AC = B(1 + C) + AC = B + AC$$

L.H.S. = R.H.S.

Statement is true :

(ii) $AB + AC + BC' = AC + BC'$

L.H.S

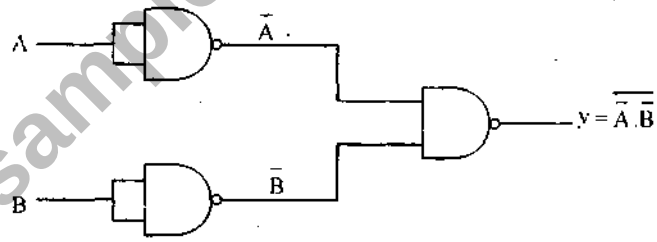
$$= AB + AC + BC'$$

L.H.S.≠ R.H.S

Statement is false

Q. 6. (b) Realize OR gate using NAND gates only and AND gate using NOR gates only. Explain your answer.

Ans. OR Gate using NAND GATE :



$$Y = \overline{\bar{A}.\bar{B}}$$

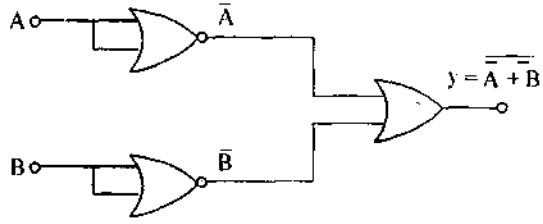
using Demorgen Theorem

$$Y = \bar{\bar{A}} + \bar{\bar{B}}$$

$$Y = A + B$$

(OR Gate expression)

(c) AND Gate using MOR Gate :



$$Y = \overline{\bar{A} + \bar{B}}$$

using Demorgen theorem

$$Y = \bar{\bar{A}}.\bar{\bar{B}}$$

$$\boxed{Y = A.B}$$

Q. 6. (c) Explain BCD numbers. How two *BCD* numbers are added ?

Ans. BCD stand for *B*inary Coded Decimal :

	BCD Number
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Addition of BCD Number : for example add $(36)_{10}$ into $(17)_{10}$ BCD Number

$36 \rightarrow 0011 \quad 0110$

$17 \rightarrow \underline{0001} \quad \underline{0111}$

$\underbrace{0100}_{4} \quad \underbrace{1101}$

$\underbrace{0101}_{5} \quad \underline{0110}$

$\underbrace{0011}_{3}$

Ans ⇒ 53

If number is greater than 1001, than add 0110 to them other wise leave that

Q. 7. Attempt any one part of the following $10 \times 1 = 10$

(a) Write the names of Non-integrating and Integrating type Digital Voltmeter. With the help of Block Diagram explain the working principle of any one of integrating type DVM. Also give the merit and demerit of technique used.

Ans. Non integrating : (1) Ramp Type DVM **(2) Intigrating Type :** Dual Slop DVM

Block Diagram of Digital Voltmeter : The main parts of the digital voltmeter system have been shown in given block diagram.

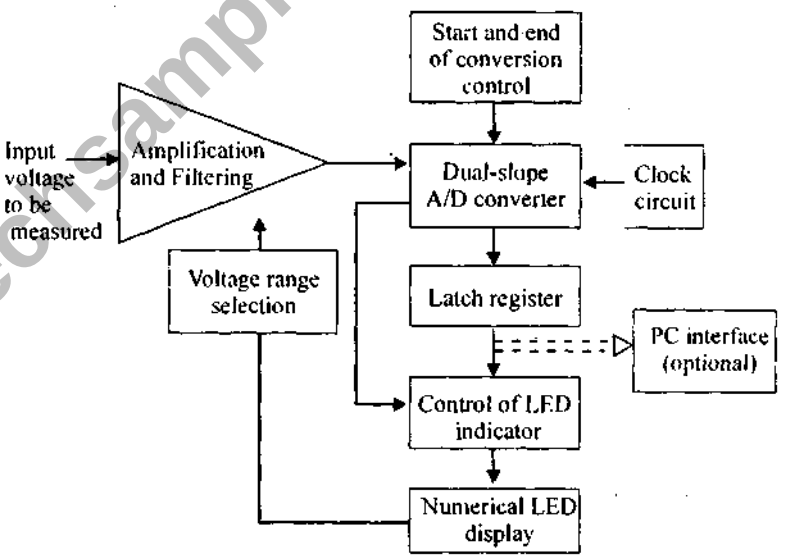


Fig. Block diagram of DVM.

The system has the following parts :

1. *Dual-slope A/D converter* : Generally applied voltage is analog. To measure and display that analog voltage, the analog to digital conversion is applied.

2. *3 voltage ranges manually selected (0-2V, 2-20 V, 20-200V)* : This function helps the user to select the appropriate range to measure the voltage accurately.

3. *Overflow range indication* : If the voltage is out of the manually selected range of voltmeter or value is out of range of voltmeter overflow indicator indicates to the user.

4. *Voltage reference 2V* : To measure any quantity, there must always be a reference. It is an inbuilt feature. This reference is calibrated as zero so that user directly able to measure his required value.

5. *Fixed integration time of 166.67 ms* : This is the time required to stale the output value stable.

6. *Clock frequency* : Every digital device requires clock to operate.

7. *13-bit BCD counter*

8. *Numeric* $3\frac{1}{2}$ *LED display*

9. *Control circuit built.*

10. *Power supplies.*

11. *Manual control :* start of the conversion and reset signal

The front panel of digital voltmeter has been shown here.

Q. 7. (b) Sketch a Cathode Ray tube used in a CRO and determine how many cycles of a 2-KHz sinusoidal are viewed if the sweep frequency is 1 KHz, 2 KHz, 4 KHz.

Ans. If sinusoidal are 2 kHz,

and (i) sweep with 1 kHz. then there will be $\frac{1}{2}$ cycle of 2 kHz.

(ii) Sweep with 2 kHz, then there will be 1 cycle of 2 kHz

(iii) Sweep with 4 kHz, then there will be 2 cycles of 2 kHz.

Cathode Ray Tube :

The cathode ray tube consists of three basic parts :

(1) *Electron gun* : This is an arrangement for producing and focussing an electron beam.

(2)

Deflecting system : This is an arrangement for deflecting the beam either electrostatically or magnetically.

(3)

Fluorescent screen : The electronic beam strikes on this part and produces visual sensation.

All the parts are shown in fig.

(1) The electron gun consists of the following parts :

(i) Cathode : When the cathode is heated, electrons are emitted due to thermionic emission.

(ii) Control grid : Compresses the electronic beam to obtain a fine pencil of beam.

(iii) Accelerating electrode : This attracts and accelerates electrons.

(iv) Anode I or focussing anode : This focusses the electronic beam in a fine spot.

(v) Anode II or accelerating anode : This further accelerates and focusses electronic beam.

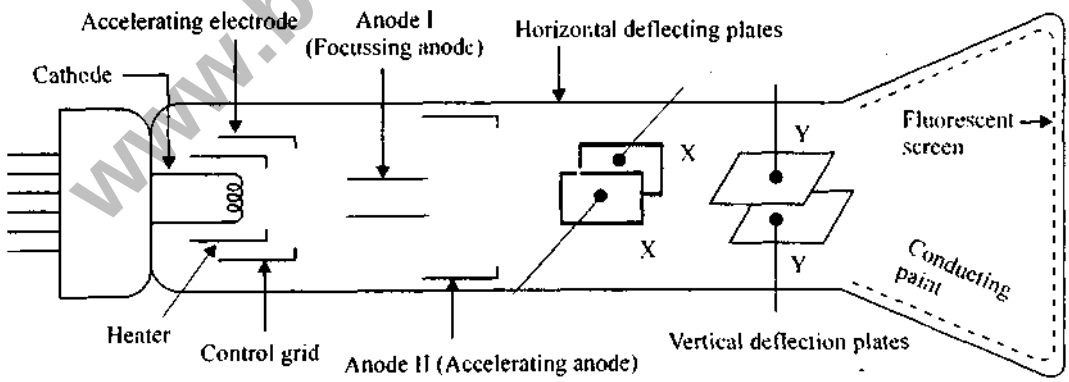


Fig.