B.Tech.

SECOND SEMESTER EXAMINATION, 2008-09

ELECTRONICS ENGINEERING

(EEC-101/EEC-201)

Time : *3 Hours]* *[Total Marks : 100*

Note : *(1) Attempt all questions.*

SECTION-A 1 × 20

1. Attempt all the parts of this questions. All parts of tbe questions carry equal marks. This question contains 20 objectives/fill in tbe blanks type/true false type questions.

(i) Diffused impurities with five valence electrons are called ..... .

(ii) In an n-type material the electron is called tbe ..... and tbe bole is ..... .

(iii) In tbe reverse bias region tbe reverse saturation current of a silicon diode doubles for energy ..... rise in temperature.

(iv) The wavelengtb and frequency of ligbt of a specific colour are directly related to tbe ..... of tbe material.

(v) In the dc mode tbe levels of I_c and I_B are related by a quantity called ..... .

(vi) The quantity Beta provides an important relationsbip between tbe base and collector current, and is usually between ..... .

(vii) For C E configuration, typical value of Zi are in the range of ..... .

(viii) Given $\beta = 150$ and $I_E = 3.2$ mA for a common emitter configuration witb $r_0 = \infty\,\Omega$, tbe value of Zi is ..... .

(ix) The input controlling variables for a BJT transistor is ..... .

(x) Tbe input impedance of all commercially available FET is ..... .

Select tbe correct answer in tbe following :

(xi) A semiconductor has a ..... .

(a) Negative temperature coeff. of resistance

(b) Constant temperature coeff. of resistance

(c) Positive temperature coeff. of resistance

(d) None of tbese.

(xii) To obtain n-type semiconductor, the impurity added to a pnre semiconductor is

(a) Trivalent

(b) Tetravalent

(c) Pentavalent

(d) None of tbese

(xiil) For a germanium PN junction tbe maximum value of barrier potential is

(a) 0.3 V

(b) 0.7 V

(c) 1.3 V

(d) 1.7 V

(xiv) The current I_{CBO} flows in tbe

(a) Emitter and base leads

(b) Collector and base leads

(c) Emitter and collector leads

(d) None of tbese.

(xv) A hiasing circuit has a stahility factor of 40. If due to temperature change, I_{co} change by 1 μA, then I_c will change hy

(a) 20 μA

(b) 40 μA

(c) 80 μA

(d) None of these.

(xvi) A zener diode has a sharp hreak-down voitage at low reverse voltage. The ahove statement is

(a) True (b) Faise

(xvii) A varactor diode is optimiged for its variahle capacitance. Above statement is

(a) True (b) False

(xviii) The most commonly used transistor circuit arrangement is common collector. The above statement is

(a) True (h) False

(xix) The emitter of a transistor is doped moderately. The ahove statement is

(a) True (h) False

(xx) The ideal value of stahility factor is 10. The above statement is

(a) True (h) False.

Ans.

(i) **donars.**

(ii) **majority carriers, minority carriers.**

(iii) **10°C.**

(iv) **refractive index (μ).**

(v) **current amplification factor β.**

(vi) **50 to 400.**

(vii) **1218.75 Ω.**

(viii) $Z_i = 1218.75\ \Omega$.

$$\left[re = \frac{26\ mV}{IE} = \frac{26\ mV}{3.2\ mA} \right.$$

$= 8.125$, $Zi = \beta re$

$= 150 \times 8.125 = 1218.75\ \Omega$]

(ix) **base current (IB).**

(x) **$10^9 \Omega$ (1000 mΩ).**

(xi) (a) Negative temperature coeff. of resistance

(xii) (c) Penta valent

(xiii) (a) **0.3 V**

(xiv) (b) Collector and base leads

(xv) (b) **40 μA**

(xvi) (a) true

(xvii) (a) true

(xviii) (b) false

(xix) (a) true

(xx) (b) false.

SECTION-B

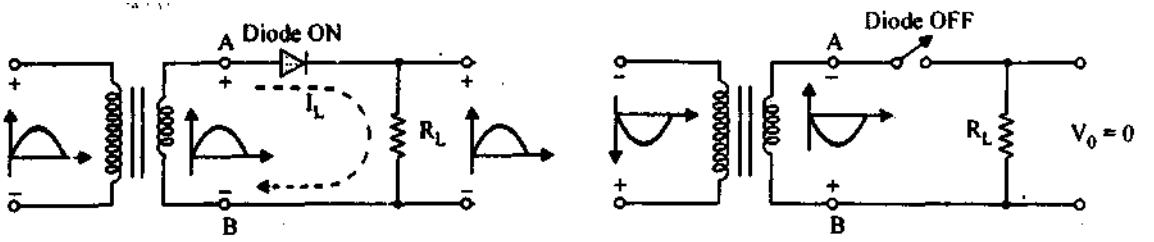
***Note* : Attempt any three parts of the following :** $10 \times 3 = 30$

Q. 2. (a) Explain the working of Half wave and Full wave bridge rectifier. What are the advantage of full wave rectifier ?

Ans. Operation of the HWR : The operstion of HWR circuit is as follows :

Operation in the positive haif cycle of as supply (0 – π) :

- In the positive half cycle (0 – π) of tbe ac supply, the secondary voltage V_{AB} is positive i.e., *A* positive with respect to *B*., Hence the diode is forward biased and starts conducting.
- The equivalent circuit of HWR for the positive half cycle is shown in Fig. (a) As the diode starts conducting, the secondary voltage



(a) Equivalent circuit for positive half cycle **(b) Equivalent circuit for negtive half cycle**

Fig.

V_{AB} appears almost as it is across the load resistance (as the voltage drop across a conducting diode is vary small).

- The load voltage is thus positive and almost equal to the instantaneous a secondary voltage V_{AB}.
- The load current has the same shape as that of the load voltage since the load is purely resistive. The waveforms for HWR are shown in Fig. (b)
- The instantaneous load current i_L is equal to the ratio of instantaneous secondary voltage (V_{AB}) and total resistance ($R_S + R_F + R_I$).

$$i_L = \frac{V_{AB}}{(R_S + R_F + R_I)} \quad ...(1)$$

Operation in the negative half cycle of ac supply (π to 2π) :

- Refer to the equivalent circuit shown in Fig. (h) In the negative half cycle of the ac supply, secondary voltage is negative, i.e. A is negative with respect to B.

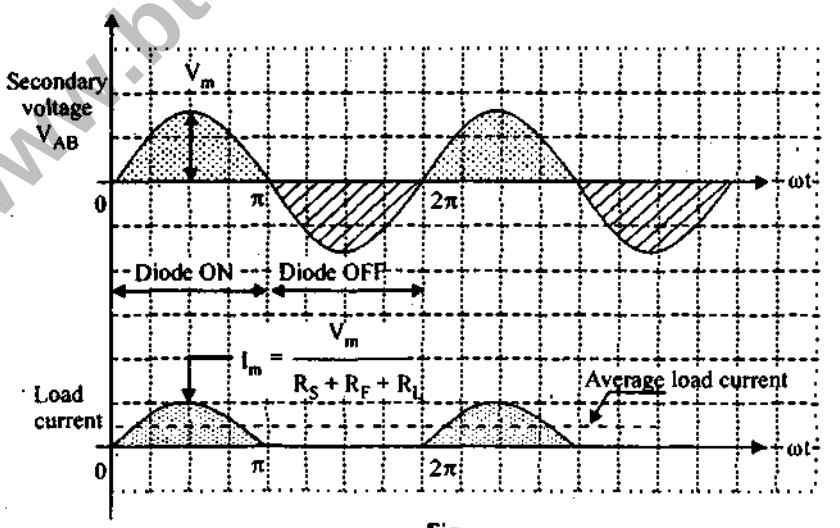


Fig.

- Hence the diode is reverse biased and offers a very high resistance. Hence we can replace it by an open circuit switch.
- The load is disconnected from the secondary. Hence the load voltage and load current both are zero and the voltage across the diode is equal to the instantaneous secondary voltage V_{AB}.The waveforms are shown in Fig.

Bride Rectifier :

- The disadvantages of the full wave rectifier such as high PIV and compulsory use of center tapped transformer are overcome in the bridge rectifier.
- The circuit configuration of bridge rectifier is as shown in Fig. It consists of four diodes connected to form a bridge.
- The center tapped input transformer is not required. The input transformer T_1 shown in Fig. is a step down transformer.
- Bridge rectifier full wave rectification. The diodes conduct i.e. at any given instant of time, one pair of diodes either D_1 D_2 or D_3D_4 will be conducting.

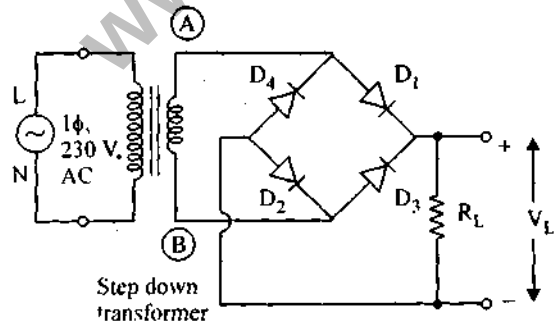
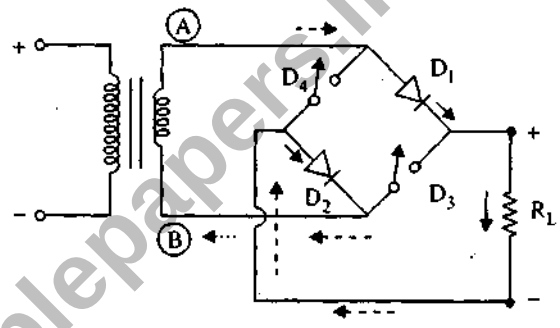
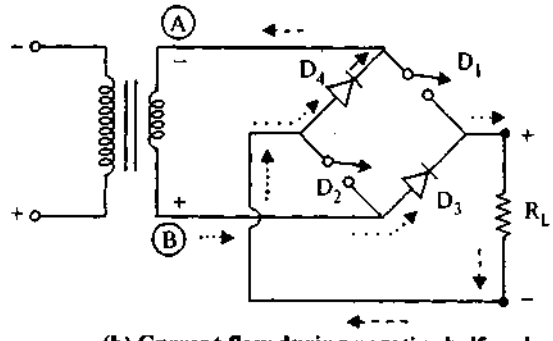


Fig. A bridge rectifier circuit

Operation of the Bridge Rectifier : Operation of the bridge rectifier can be explained in two half cycles of the AC supply voltage as follows.



(a) Current flow during positive half cycle



(b) Current flow during negative half cycle

Fig.

(i) Operation in the positive half cycle ($0 \le \omega t \le \pi$) :

- In the positive half cycle of the ac supply the secondary voltage V_{AB} is positive. Therefore diodes D_1 and D_2 are forward biased whereas D_3 and D_4 are reverse biased.

- The equivalent circuit for this interval is as shown in Fig. Note that the revers biased diodes D_3 and D_4 act as open switches.

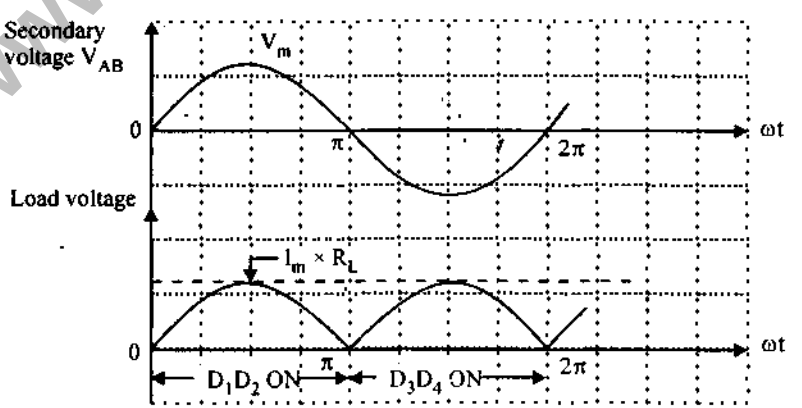
The load current and load voltage both are positive as shown in the waveforms in Fig.

(ii) Operation in the negative half cycle ($\pi \leq \omega t \leq 2\pi$)

- In the negative half cycle of the ac supply the secondary voltage V_{AB} becomes negative. Diodes D_3 and D_4 are forward biased and start conducting.
- D_1 and D_2 are reverse biased hence do not conduct. The equivalent circuit for this interval is as shown in Fig. (b).
- The waveforms of the bridge circuit are as shown in Fig.

Advantages of Bridge Rectifier :

1. It requires a small size transformer. Center tap transformer is not required. This makes the bridge rectifier cost effective.
2. The input transformer is not a must. It is possible to operate the bridge rectifier directly on the 230 V ac supply.
3. This circuit is most suitable for the high voltage applications. This is because the maximum negative voltage that appears across each diode is $-V_m$. Therefore the diodes with PIV rating of $-V_m$ Volts are required to be selected. (PIV in full wave rectifier is $-2V_m$).
4. Core saturation does not take place. Therefore transformer losses are reduced. Core saturation is avoided because equal and opposite currents flow through the transformer in each cycle.
5. The PIV is only V_m volts which is half the PIV of full wave rectifier with center tap.
6. High average output voltage.
7. Rectifier efficiency η is high.
8. Transformer utilization factor TUF is high.



Q. 2. (h) A half wave rectlfier ls used to snpply 10 V d.c. to a reslstive load of 400 Ω. If the crystal diode has a forward resistance of 20 Ω . Determine the valne of a.c. voltage supplied to the circult.

Ans. given $V_{dc} = 10$ $R = 400\ \Omega$, $R_f = 20\ \Omega$

$$V_{dc} = \frac{V_m}{\pi}$$

$$V_m = V_{dc} \times \pi$$

$$= 10 \times 3.14$$

$$= 31.4$$

$$\text{Now } I_m = \frac{V_m}{R + R_f}$$

$$= \frac{31.4}{400 + 20}$$

$$= .0523 \text{ smp}$$

$$I_{rms} = \frac{I_m}{2} = \frac{0.523}{2} = .0261 \text{ amp}$$

$$\text{Pinket} = (I_{rms})^2 (R_L + R_f)$$

$$= (0.261)^2 (400 + 20)$$

$$= .28 \text{ watt.}$$

Q. 2. (c) Explaln the potential dlvider hiasing circuit.

Ans. This is the third bias stabilizing circuit. The circuit disgrsm of voltage divider bias is ss shown in Fig.

Features of the circuit :

- The resistors R_1 and R_2 form a potential divider to apply a fixed voltage V_B to the base.
- A resistance R_E has been connected in the emitter circuit.This resistor is not present in the fixed bias or collector to base bias circuits.

Blas stahillzatlon using voltage divider hias circuit :

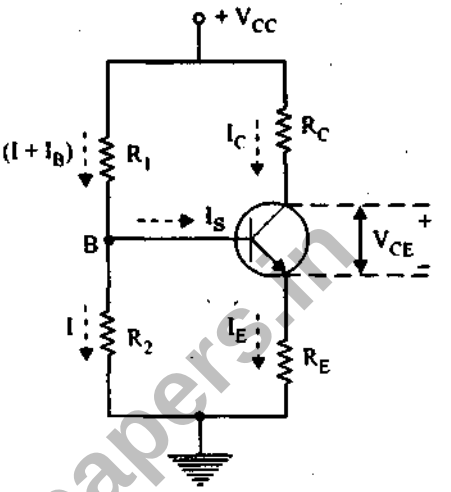


Fig. Voltage divider bias

- If I_C increases due to change in temperature or β_{dc}
  ⇓
- Then I_E increases
  ⇓
- Hence drop across R_E increases ($V_E = I_E R_E$)
  ⇓
- But V_B is constant. Hence V_{BE} decreases
  ⇓
- Hence I_B decreases
  ⇓
- Hence I_C also decreases. Thus the compensation for increase in I_C is achieved.

Exact Analysis using Thevenin's Equivalent Circuit :

- If the condition $I_B <<< I$ is not satisfied by the self bias circuit then the exact analysis should be performed.

- The procedure to be followed for the exact analysis is as follows.

Procedure for exact analysis

Step 1 : Draw the Thevenin's equivalent of self bias circuit.
Step 2 : Obtain I_B by applying KVL to the base loop.
Step 3 : Obtain $I_C = \beta I_B$
Step 4 : Obtain the expression for V_{CE} by applying KVL to collector loop.

Step 1 : Thevenin's equivalent circuit :

The Thevenin's equivalent circuit of the voltage divider bias circuit is as shown in Fig. The resistances R_1 and R_2 are replaced by R_B and V_{TH}' where V_{TH} is the Thevenin's voltage and R_B is the parallel combination of R_1 and R_2.

$$\therefore \quad R_B = \frac{R_1 R_2}{(R_1 + R_2)} \qquad ...(1)$$

$$\text{and } V_{TH} = \frac{R_2 V_{CC}}{(R_1 + R_2)} \qquad ...(2)$$

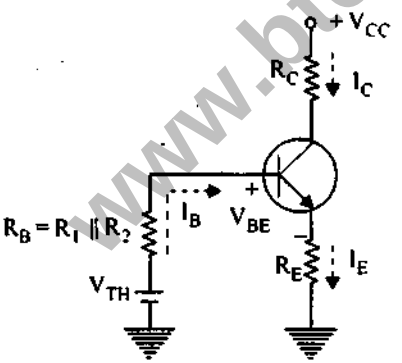


Fig. Thevenin's equivalent circuit for voltage divider bias.

Step 2 : Obtain the expression for I_B :

Applying KVL to the base loop of Fig we get,

$$V_{TH} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\therefore V_{TH} - I_B R_B - V_{BE} - (1 + \beta_{dc}) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_B + (1 + \beta_{dc}) R_E} \qquad ...(3)$$

This is the required expression for I_B.

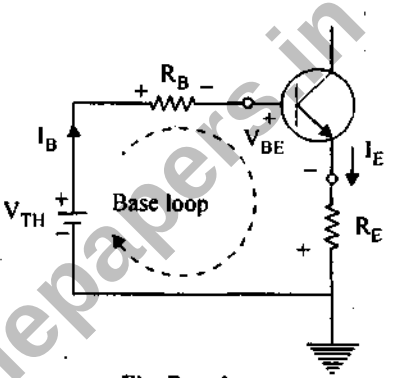


Fig. Base loop

Step 3 : Obtain expression for I_C:

$$I_C = \beta_{dc} \times I_B = \frac{\beta_{dc} (V_{TH} - V_{BE})}{R_B + (1 + \beta_{dc}) R_E} \qquad ...(4)$$

Step 4 : Obtain tbe expression for V_{CE} :

Apply KVL to the collector loop shown in Fig. to get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

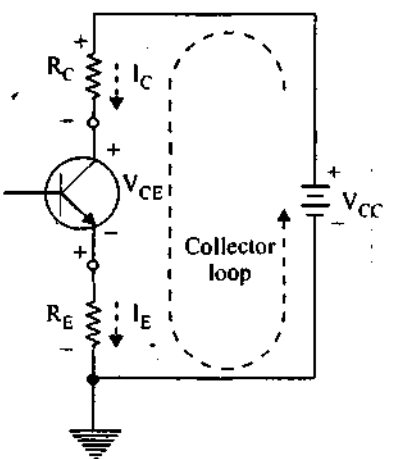


Fig. Collector loop

$\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E$ ...(5)

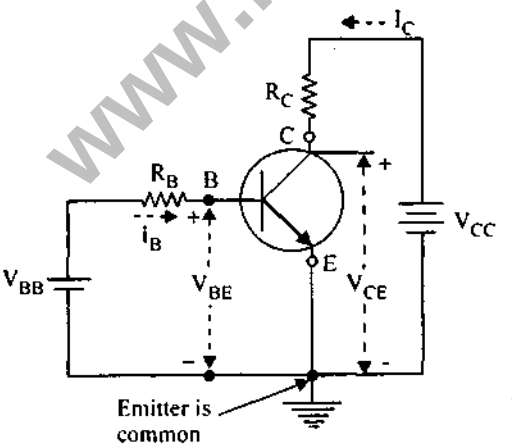
This is the required expression for V_{CE}.

Q. 2. (d) Explain the CE and CC configuration of BJT.

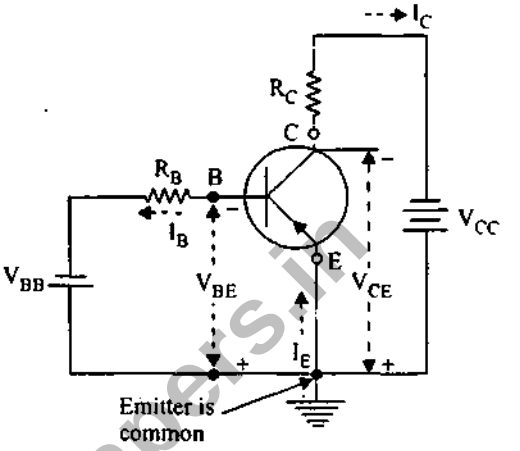
Ans. The common emitter configuration for the p-n-p and n-p-n transistors is as shown in Figs. (a) and (b).

The important points about the CE configuration are as follows :

- Now the emitter acts as a common terminal between input and output.The input voltage is applied between base and emitter. Hence V_{BE} is the input voltage and I_B is the input current.
- The output is taken between the collector and emitter.Therefore V_{CE} is the output voltage and I_C is the output current.
- In order to operate the transistor in its active region, the base-emitter (BE) junction is forward biased and the collector base junction is reverse biased.



(a) Common emitter configuration for o-p-n transistor

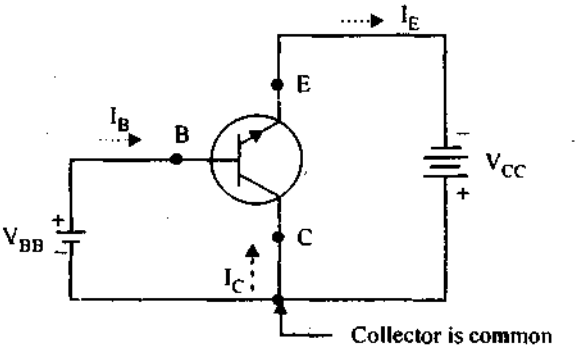


(b) Common emitter configuration for p-n-p transistor

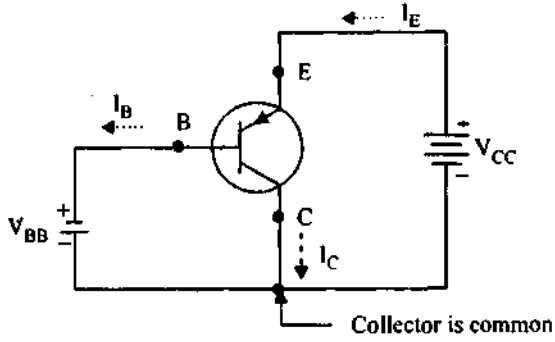
Fig.

Common Collector (CC) Configuration :

- The common collector (CC) configuration for p-n-p and n-p-n transistors is as shown in Fig. (a) and (b).
- In the common collector configuration, the collector is made common to both input and output.
- The V_{BC} is input voltage and I_B is the input current whereas V_{EC} is the output voltage and I_E is the



(a) Common collector configuration for n-p-n for transistor



(a) Common collector configuration for p-n-p for transistor

Fig.

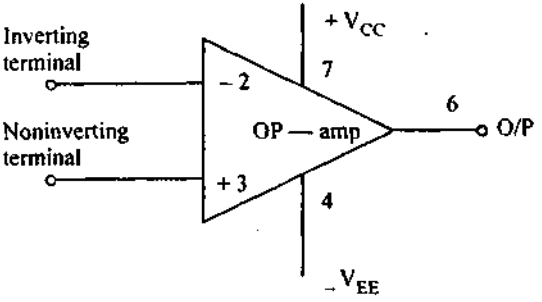
output current.This configuration is also known as "emitter follower" configuration.

- The common collector configuration is used primarily for impedance matching purpose because it bas a high input impedance and low output impedance as compared to the CB and CE configurations.

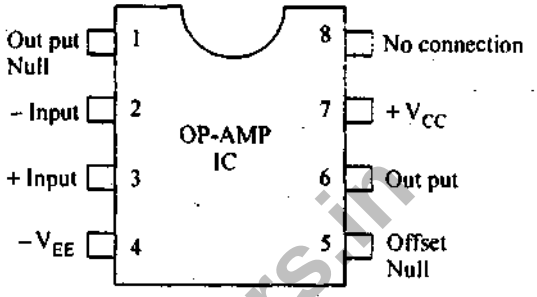
Q. 2. (e) What is OPAMP ? How it is uaed as an integrator and aummer ?

Ans. Operational amplifier (op-amp) : An op-amp is an active circuit element designed to perform mathematical operation of addition, subtraction multiplication, division, differentiation and integration in addition to amplification. So named operational amplifier (op– amp).

Block diagram :



Pin diagram :



V_1, V_2 and V_3 are three input signal applied simultaneously to inverting terminal of op–amp through resistor R_1, R_2 and R_3 respectively.

In concept of vertual ground

$$V_d = 0$$

$$\Rightarrow V_1 - V_2 = 0$$

$$\Rightarrow \quad V_1 = V_2$$

since $V_1' = 0$ so V_2' is also zero

now $I_1 + I_2 + I_3 = I_f$

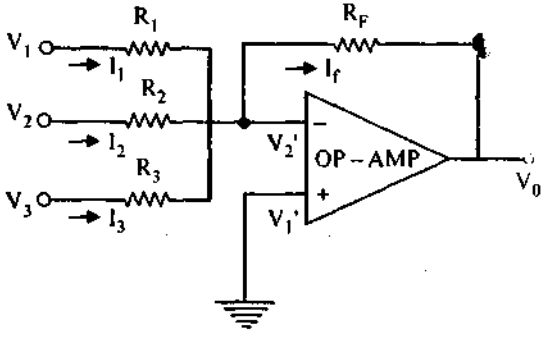
$$\frac{V_1 - V_2'}{R_1} + \frac{V_2 - V_2'}{R_2} + \frac{V_3 - V_2'}{R_3} = \frac{V_2^1 - V_0}{R_f}$$

since $V_2' = 0$

So $\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_0}{R_f}$

$$V_0 = -R_f\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

$$\boxed{V_0 = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]}$$

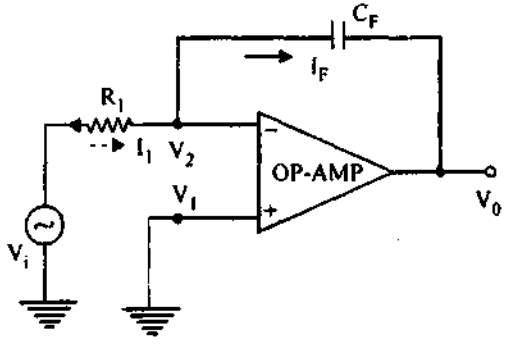


let $R_1 = R_2 = R_3 = R$

$V_0 = -(V_1 + V_2 + V_3)$

So circuit behavea or a adder or summing amplifier.

Integrator : Integrator is obtained by replacing the feed back resistor R_F in the inverting amplifier by C_F



from concept of vertual ground

$$Vd = 0$$

$$\Rightarrow \quad V_1 - V_2 = 0$$

$$[q = cV,\ idt = c.dv,\ i = c.\frac{dv}{dt}]$$

$$V_1 = V_2$$

$V_2 = 0 \quad \Rightarrow \quad V_1 = 0$

So $I_1 = I_F$

$$\frac{V_i - V_1}{R_1} = c.\frac{d}{dt}(V_1 - V_0)$$

that $V_1 = 0$

so $$\frac{V_i}{R_1} = -c\frac{d}{dt}(V_0)$$

$$\boxed{V_0 = -\frac{1}{R_1 c}\int v_i\, dt}$$

So output voltage is the integration of input voltage and circuit works as a integrator.

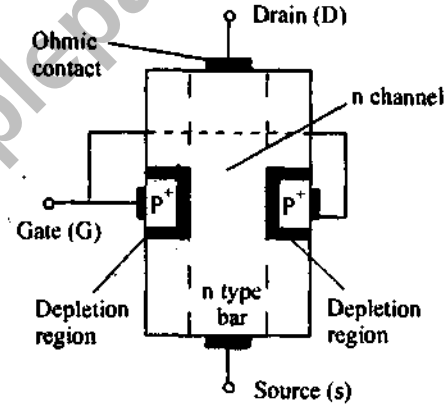
SECTION-C $10 \times 5 = 50$

Note : **Attempt all the queations. All questiona carry equal marka.**

Q. 3. Attempt any one part of the following :

(a) Explain the conatruction and characteriatica of JFET.

Ans. Construction : A n-channel JFET consist of n type silicon bar. On both side of n type bar heavily dopped p^+ region have been formed by diffusion process. So two p-n junction is formed and connected internally via a gate terminal. Other terminal are source and drain taken out from the bar.The bar forms the conducting channel for charge carriers (electron).



JFET characteristics : JFET has two charecteristics

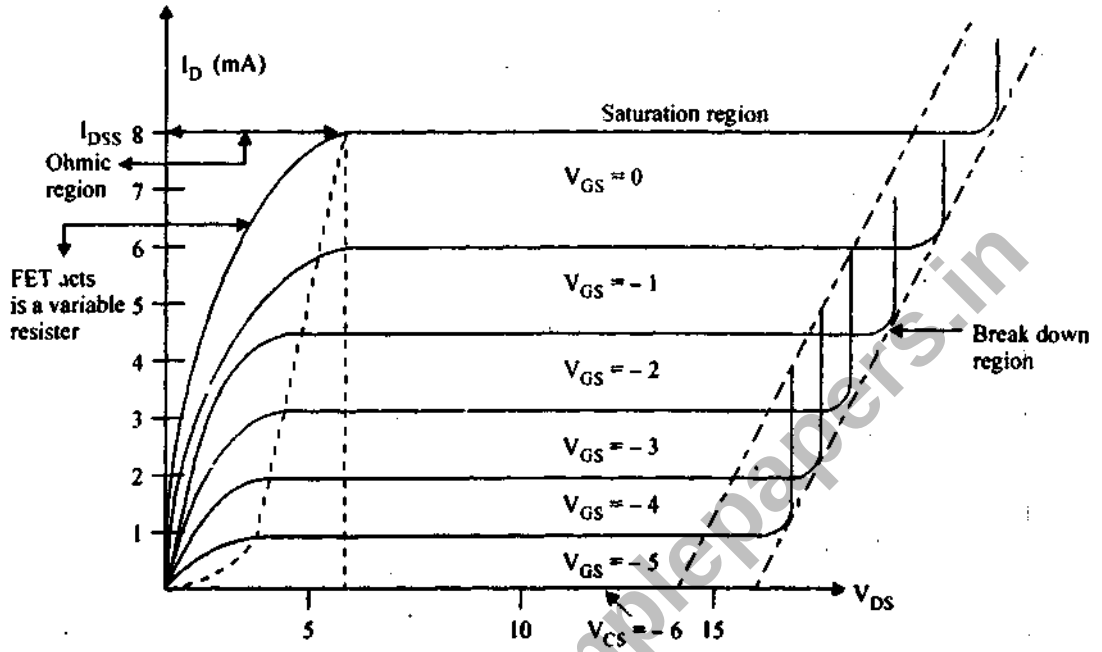
(i) Drain characteristics or output characteristics

(ii) Tranaiator charactaristics.

(I) Drain oharacteristios : It is the curve between I_D and V_{DS} for different value of V_{GS} Drain characteristics has three regions

(i) Ohmic region : Current I_D increases sharply with increase in V_{DS}.

(ii) Saturation region : I_D is constant and will not change with increase in V_{DS}.

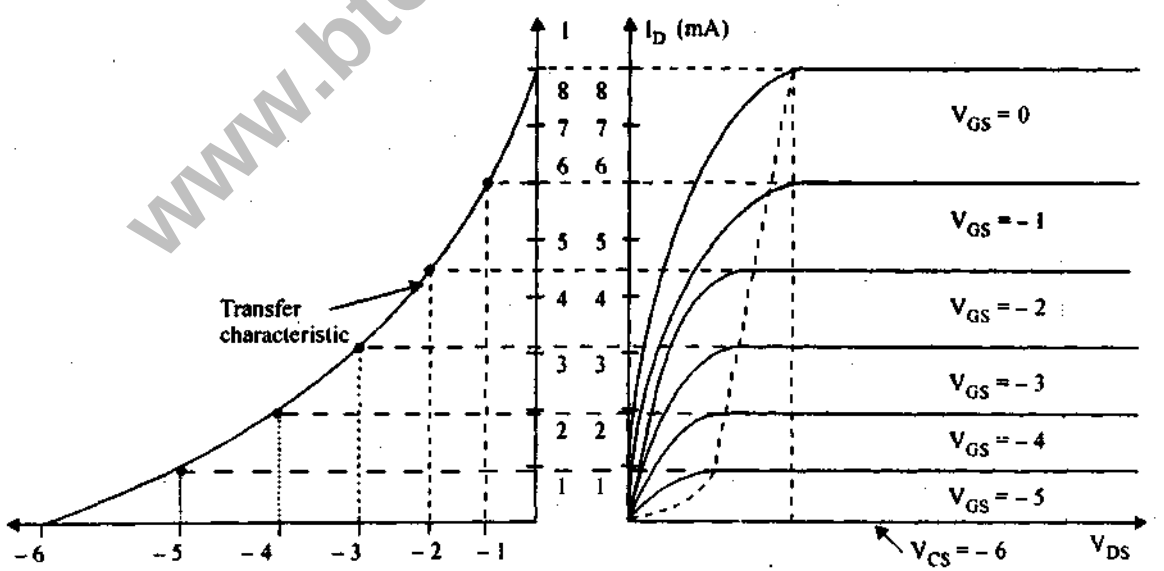


(iii) Break down region : In this region junctions are break down and I_D becomes vertical.

(II) Transfer Characteristics : It is the curve between drain current (I_D) and gate to source voltage V_{GS}. I_D and V_{GS} are related by shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{VP}\right)^2$$

where I_D : drain current



I_{DSS} : drain to source saturation current

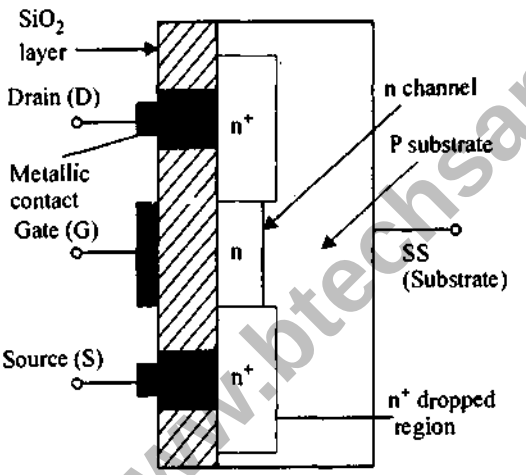
V_{GS} : gate to source voltage (negative)

V_P : Pinch off voltage (negative)

Transfer characteristics are obtained from obtain characteristic.

Q. 3. (b) Explain the basic construction, operation and characteristics of MOSFET.

Ans. Construction : The substrate used is p type silicon material. It serves as the foundation on which the device will be constructed. The gate; drain and source are connected with metallic contact. Gate is insulated from n-channel by a very thin layer of SiO_2.

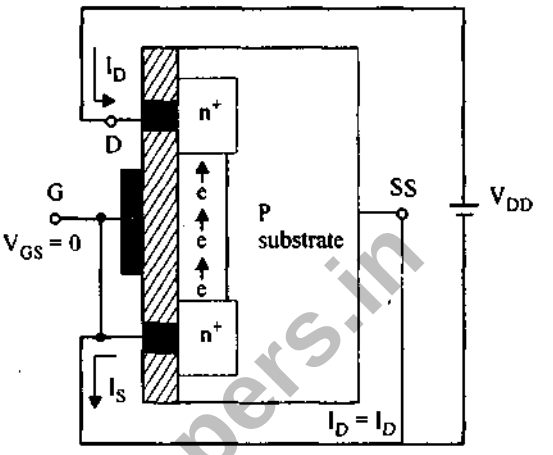


Construction

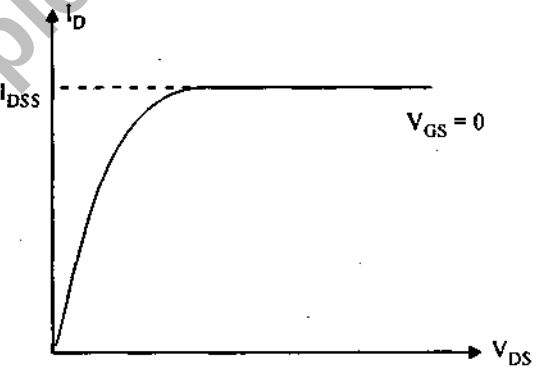
Operation :

(i) Let V_{GS} is zero and a positive V_{DS} is applied between drain and source *i.e.* $V_{GS} = 0$ $V_{DS} > 0$. In this condition free electrons of n channel moves from source to drain so current I_D flow normally.

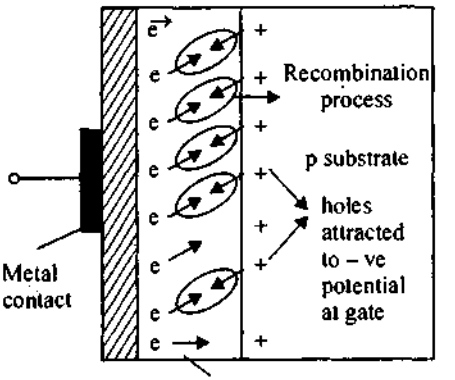
(ii) Now V_{GS} is set at a negative potential i.e. $V_{GS} < 0$ $V_{DS} > 0$.



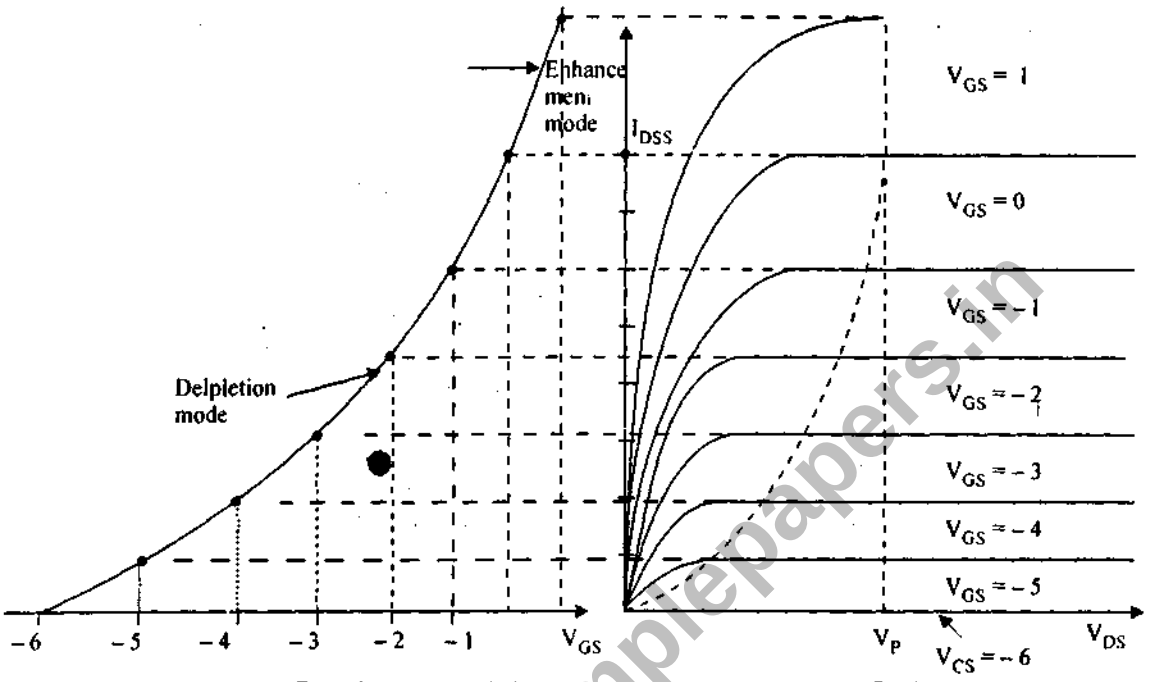
The negative potential at gate rebell the electrons of n-channel towards the p type



substrate and attract the holes from p type substrate. So recombination will occur which



Electron rebelled by negative potential at gate



will reduce the number of electron in channel. So drain current decreases. As the negative potential at gate is increased the rate of recombination increase. So the resulting level of drain current decreases.

(iii) Now V_{GS} is set at a positive potential i.e. $V_{GS} > 0, V_{DS} > 0$

In this condition the positive voltage of gate will draw additional electron from p type substrate. So electron in channel increases so I_D increases.

Characteristics of n depletion MOSFET : It has two type of characteristics

(i) drain or output characteristics.

(ii) Transfer characteristic.

So Depletion MOSFET can work in Depletion and Enhancement mode both for Depletion V_{GS} is negative and for Enhancement V_{GS} is positive.

Q. 4. Attempt any one part of the following :

(a) (i) Convert the $(725.25)_{10}$ to its equivalent in Base-2, Base-8 and base-16

Ans. (I) $(725.25)_{10}$ to base -2

Integer Part

	Q	R
2	725	
2	362	1
2	181	0
2	90	1
2	45	0
2	22	1
2	11	0
2	5	1
2	2	1
	1	0

Fractional part

$.25 \times 2 = .05$

$.5 \times 2 = 1.0$

$\therefore (.25)_{10} = (.01)_2$

So, $(725.25)_{10}$

$= (1011010101.01)_2$

$\therefore (725)_{10} = (1011010101)_2$

$(725.25)_{10}$ to base -8

Integer Part **Fractionai part**

	Q	R
8	725	
8	90	5
8	11	2
	1	3

$.25 \times 8 = 2.00$

$\therefore (.25)_{10} = (0.2)_8$

$\therefore \quad (725)_{10} = (1325)_8$

$\therefore (725.25)_{10} = (1325.2)_8$

Integer Part **Fractional part**

	Q	R
16	725	
16	45	5
	2	13 (D)

$.25 \times 16 = 4.00$

$\therefore \quad (.25)_{10} = (0.4)_{16}$

$\therefore (725.25)_{10} = (2D5.4)_{16}$

$\therefore (725)_{10} = (2D5)_{16}$

(ii) Perform M-N and M+N if M = 10101 and N = 1111.

Ans. M – N here M= 10101

N = 011 H

10101
-01111
00110 **Ans.**

M + N

10101
+01111
100100 **Ans.**

Q. 4. (b) Discuss the postulates of booiean algebra. How it is different from ordinary algebra ? What are universal gates ?

Implement the expression of XOR gate witb tbe beip of NAND gates only

Ans. The rules of Boolean Algebra are different from those of the conventional Algebra in the following manner :

1. Symbols used in Boolean algebra (usually letters) do not represent numerical values.
2. Arithmetic operations (addition, subtraction , division etc.) are not performed in boolean algebra. Also there are no fractiona, negative numbers, square, square root, logarithms imaginary numbers etc.
3. Third and most important point is Boolean Algebra allowa only two possible values ("0" to "1") for any variables.

Boolean Postulates

(i) Commutative Law :

Any binary operation which satisfies the following expression is referred to as commutative operation :

1. $A . B = B . A$
2. $A + B = B + A$

Thus the commutative law states that changing the sequence of the variables (inputs) does not have any effect on the output of a logic circuit.

(ii) Associative Law :

This law states that the order in which the logic operations are performed is irrelevant as their effect is the same.

i.e. $(A . B) . C = A . (B . C)$

and $(A + B) + C = A + (B + C)$

Similarly we can verify the other statament i.e.

$A + (B + C) = (A + B) + C$

(iii) Distributive Law :

This distributive law states that,

$A . (B + C) = AB + AC$

(iv) AND Laws :

These laws use the AND operation therfore they are called as "AND" laws. The AND laws are as follows :

1. $A . 0 = 0$ i.e. ANDing with a 0, always results in output
2. $A . 1 = A$ i.e. ANDing of A with a, 1 results in A.

3. $A \cdot A = A$ i.e. ANDing of an input with itself will produce the same output
4. $A \cdot \overline{A} = 0$ i.e. ANDing of an input with its complement results in a 0 output.

(v) OR Laws :

These laws use the OR operation. Hence they are called as OR laws. The OR laws are as follows :

1. $A + 0 = A$ i.e. ORing an input with 0, results in the output equal to input.
2. $A + 1 = 1$ i.e. ORing an input with 1, always results in a high output.
3. $A + A = A$ ie. ORing an input with itself, results in the same output
4. $A + \overline{A} = 1$ ie. ORing an input and its complement always results in a high output.

(vi) Inversion Law :

This law uses the "NOT" operation. The inversion laws ststes that double inversion of a variable results in the original variable itself i.e.

$$\overline{\overline{A}} = A$$

Universal Gates :

- The NAND and NOR gates are called as "Universal Gates" because it is possible to implement any Boolean expression with the help of only NAND or only NOR gates.
- Hence a user can build any combinational circuit with the help of only NAND gates or only NOR gates.
- The symbol of a two input NAND gate is shown in Fig. (a) where a bubble (o) on the output side represents inversion.
- The truth table of a two input NAND gate is shown in Fig. (c), which shows that the output is low (0) if and only if both the inputs are high (1) simultaneously. For all other input combinations the output voltage with be high (1).
- A NAND gate is called as "Universal Gate" because we can construct AND, OR and NOT gates using only NAND gates.

EX OR gate naing NAND :

- The Boolean expression for EX-OR gate is
  $Y = A \oplus B = \overline{A}B + A\overline{B}$
- Taking double inversion of RHS,
  $Y = \overline{\overline{\overline{A}\,B + A\,\overline{B}}}$
  Let $X = \overline{A}B$ and $Z = A\overline{B}$ $\therefore Y = \overline{\overline{X + Z}}$
- Using De Morgan's theorem $\overline{X + Z} = \overline{X} \cdot \overline{Z}$

$\therefore Y = \overline{\overline{X} \cdot \overline{Z}} = \overline{(\overline{A}B) \cdot (A\,\overline{B})}$

- This is the required expression for EX-OR using only NAND. Fig. shows the realization.

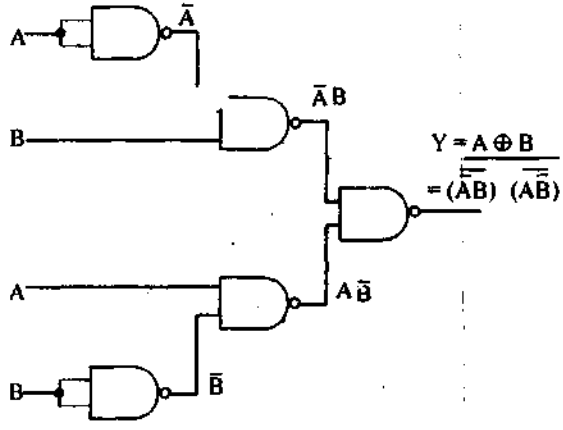


Fig. EX-OR using NAND gates

Q. 5. Attempt any one part of the following :

(a) Simplify the boolean fnnction F in sum of products using don't care conditions d (using K-map)

(i) $F = Y' + X'Z'$

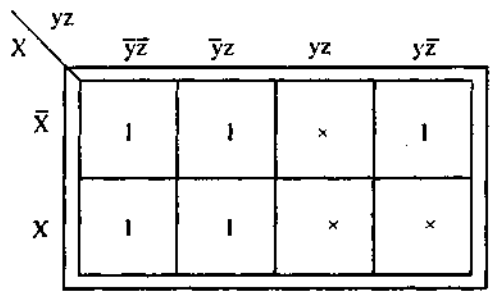
$d = YZ + XY$

(ii) $F = B'C'D' + BCD' + ABCD'$

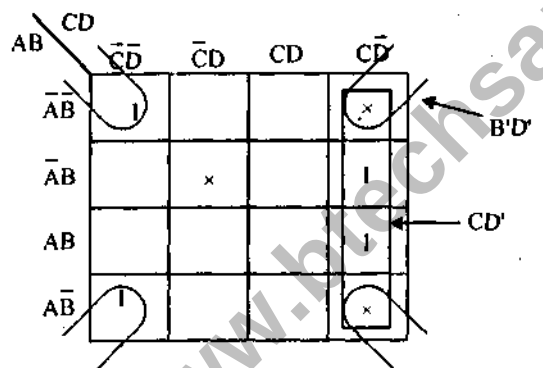
$d = B'CD' + A'BC'D$

Ans. (i) $F = Y' + X'Z'$

$d = YZ + XY$



So F = 1



(ii) $F = B'C'D' + BCD' + ABCD'$

$d = B'CD' + A'BC'D$

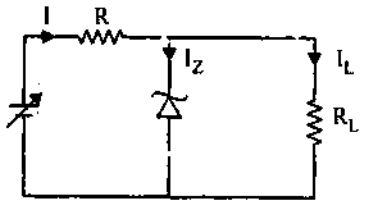
So $F = B'D' + CD'$

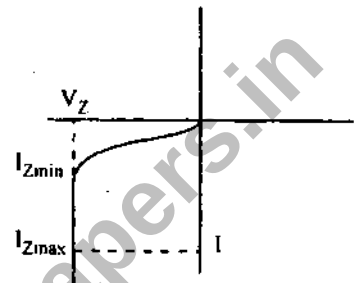
$= D'(B' + C)$

Q. 5. (b) How zener diode is used as shunt regulator ? Explain it.

Ans. Zener diode or a Sbunt regulator : Zener diode can be used as a voltage regulator i.e. it is provide constant voltage when operated in reverse bias.

(i) Input voltage is varying and load is constant .





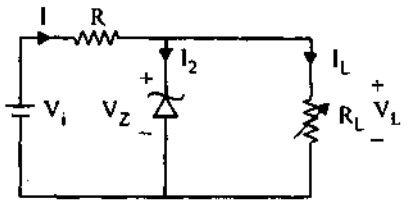
If V_i is increased then I will increase

$$\uparrow I = \frac{\uparrow V_i - V_Z}{R}$$

$$I = I_L + I_Z$$

V_Z is constant and R_L is also constant.

So I_L is constant so increase in I will increase the zerner current but it should be less than I_Z max. So diode operates in zener region and of O/P voltage is constant.



If V_i is decreased then I will decrease

$$\downarrow I = \downarrow \frac{V_m - V_Z}{R}$$

$$I = I_L + I_Z$$

V_Z is constant and R_L is constant so

I_L is constant. So I_Z is decrease but it should be greater than I_Z min. So diode operate in zener region and o/p voltage remains constant.

(ii) Load is varying and input voltage is constant.

If R_L is increased then I_L will decrease

$$\downarrow I_L = \frac{V_L}{R_L} \uparrow$$

but $I = I_2 \uparrow + I_L \downarrow$

$\swarrow$

constant

I should be constant as V_i is constant so I_2 will will increase but if should be less than $I_{Z\max}$. So diode operates in zener region and output voltage remains constant.

If R_L decreases then I_L increases

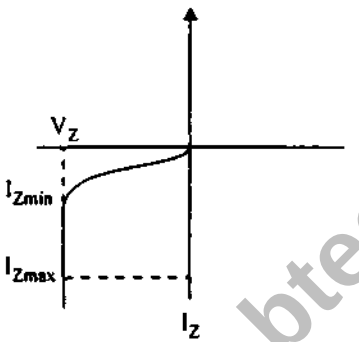
$$\uparrow I_L = \frac{V_L}{R_L \downarrow}$$

Now, $I = I_2 \downarrow + I_2 \uparrow$

$\swarrow$

constant

I is constant as V_i is constant so I_Z will increase. But it should be less than $I_{Z\min}$. So diode operates in zener region and output voltage remains constant.



6. Attempt any one part of the following :

(a) Explain the working of digital multimeter. What are its application ?

Ans. Digital Multimeter (DMM) ; A DVM can measure only the voltage but DMM can measure following quantities :

(i) Ac. or dc. voltage (ii) Ac or dc. current (iii) Resistance

In addition the these DMM can also be used to test capacitor diode, resistor.

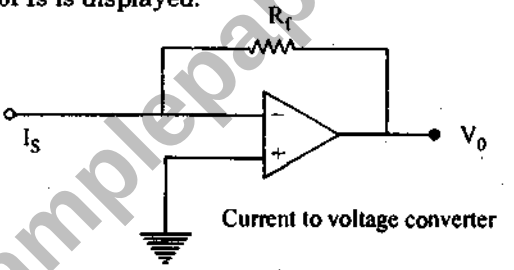
In DMM all quantities (except to voltage) are first converted into equivalent d.c. voltage by some device block diagram.

(i) Measurement of voltage : DC voltage is measured or in DVM for measurement of ac voltage the I/p a.c voltage is first converted to D.c. voltage by rectifier and then applied of DVM.

(ii) Measurement of Current ; for measurement of current a current to voltage converter is sued

$$\boxed{V_0 = -I_s R_f}$$

where R_f is known resistance and I_s is unknown current (to be measured).The output voltage V_0 is proportional to source current I_s is applied to DVM section of DMM and value of Is is displayed.

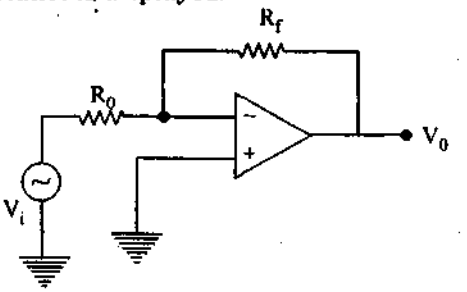


(iii) Measurement of resistance : The DMM measure the resistance by applying a known current from constant current source to unknown resistance (to be measured).Then digitizing the resultant voltage develop.

v_i, R_i is known and R_f is unknown

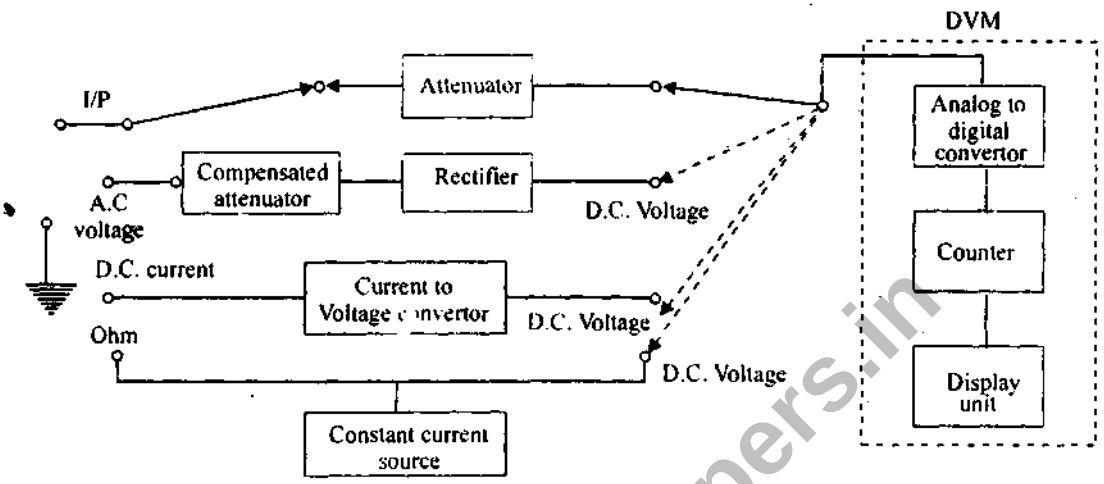
$$\boxed{v_0 = -\frac{R_f}{R_i} v_i}$$

So V_0 is proportional to R_f is applied to DVM section of DMM and value of unknown resistance is displayed.



Specification :

(i) Range : D.C. Voltage up to 1000 V



A.C. Voltage up to 250 V
D.C. Current up to 10 A
A.C. Current up to 10 A
Resistance upt to 200 M Ω

(ii) Accuracy :

.5% for dc voltage
1% for A.c voltage
1% for dc current
1.2% for ac current
.3% for resistance

(iii) Display : $3\frac{1}{2}$ digit, LCD

(iv) Power supply : 9V Battery

Q. 6. (b) Discuss in detail CRO. How is used for measurement of frequency ?

Ans. Cathode ray oscilloscope : The CRO is very useful and versatile device or laboratory instrument used for display, measurement and analysis of waveform.

(i) Vertical amplifier : The input signal is applied to vertical amplifier. This is called as vertical amplifier because it's output is applied though the delay line to the vertical deflection plates. The vertical amplifier is necessary to amplify weak signal.

Vertical amplifier is a broad band amplifier (band width is large) in order to amplify input signal over wide range of frequencies. **So the bandwidtb of CRO is decided by the vertical amplifier.**

Output of vertical amplifier is also applied to the trigger circuit for triggering the time base generator.

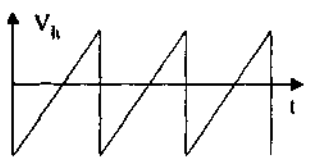
(ii) Delay line : If delay line is not used then the amplified input signal would be passed to vertical plates directly.

However the signal in horizontal section will have to pass through a trigger circuit, time base generator and horizontal deflection plates. Due to this the signal in the horizontal section will reach the horizontal plates slightly late as compared to the signal reaching the vertical plates.

If we do not compensate for this delay. Then a part of the signal will be lost. Therefore a delay line is used to delay the signal applied to vertical plates. This will ensure that the signal horizontal and vertical plates arrive exactly the same instant of time.

(iii) Trigger Circuit : The trigger circuit ensure that horizontal sweep signal starts at the same point of the input signal in every sweep. This circuit generates trigger pulses to turn on the time base circuit in every sweep.

(iv) Time base generator : The time base generator generates a saw tooth voltage waveform and applied it between the horizontal deflection plates.



Saw tooth waveform

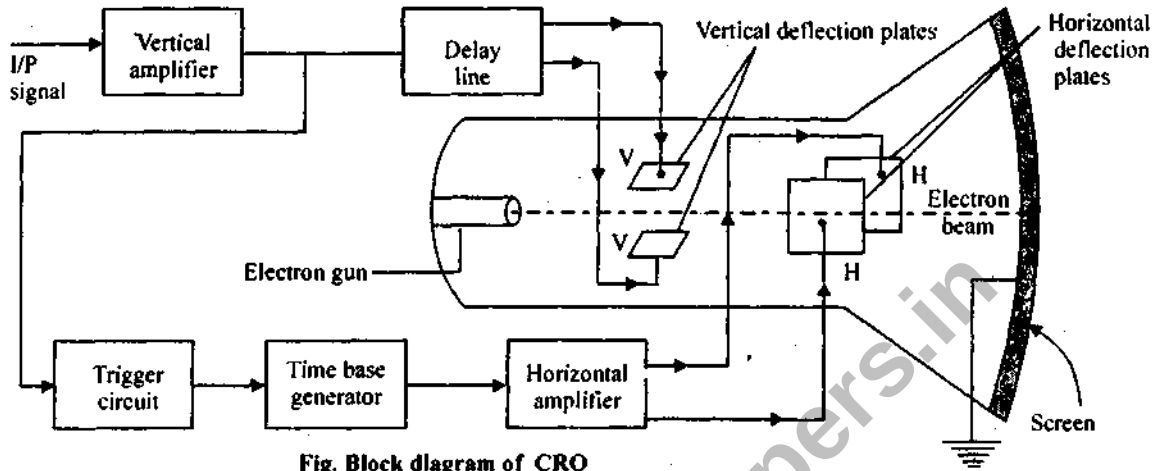


Fig. Block diagram of CRO

Horizontal amplifier : The strength of the saw tooth signal available at the output of time base generator is not sufficient.Therefore a horizontal amplifier is used to amplify the signal and apply it to the horizontal deflection plates.

Measurement of freqnency :

The steps to be followed for the frequency measurement are :

(i) Count the number of division in horizontal direction corresponding to one cycle of the waveform.
The number of division is 4.

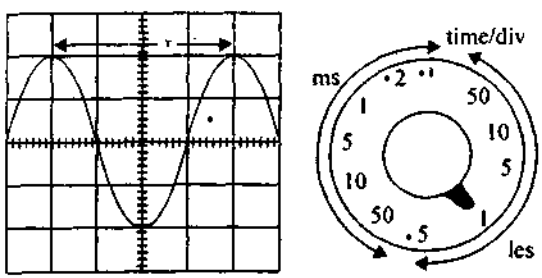
(ii) Read the position of tim/div control.
It is at 1 μs/div

(iii) Calculate the time T of one complete cycle as :

T = number of division × Time/div
$= 4 \times 1\,\mu s = 4\,\mu s$

(iv) Calculate the frequency of displayed signal

$$f = \frac{1}{T} = \frac{1}{4 \times 10^{-6}} = .25 \times 10^{+6}$$



f = 250 KHZ

Q. 7. Attempt any one part of the following :

(a) Explain the working of positive clipper and negative clamper circuits.

Ans. Positive Clipper : A positive clipper removes the positive half cycle of the input voltage waveform. These are of two type.

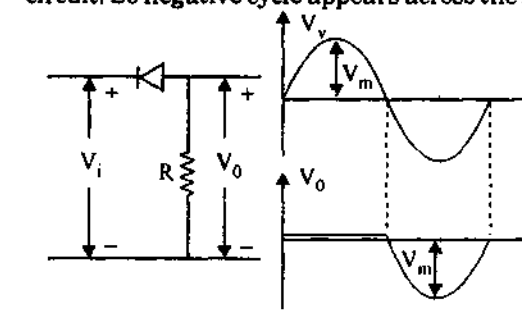
(a) Series positive clipper

(b) Shunt positive clipper

(a) Series positive clipper :

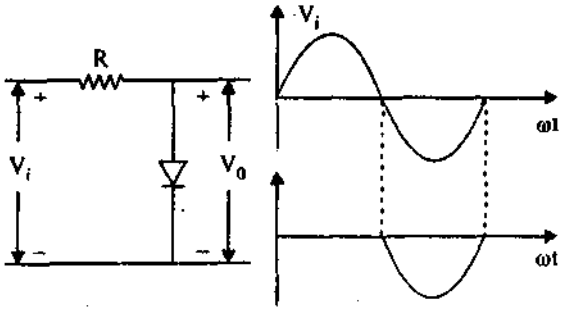
Operation : During positive half cycle of input signal diode is revers biased. So diode will not conduct and acts as open circuit. So o/p will be zero.

During negative half cycle of input signal diode is forward biased and acts as a short circuit. So negative cycle appears across the load.



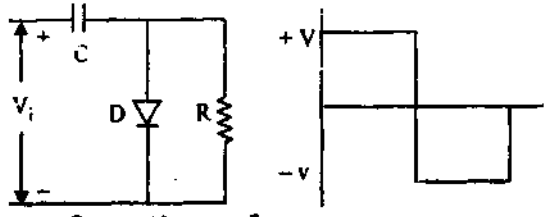
(b) Shunt of parallel Clipper

During positive half cycle of input signal diode is forward biased an acts as a short circuit. The output across the short ckt. will be zero.

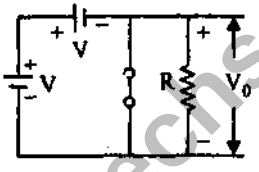


During negative half cycle of input signal diode is reverse biased and acts as a open circuit. So negative cycle appear across the load.

Negative clamper : It clamps the input waveform in downward direction.



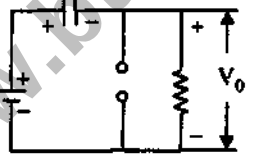
Operation : In positive cycle diode is forward biased and act as short ckt. So capacitor is quickly charged to voltage because charging time constant is very low.



$$V - V - V_0 = 0$$

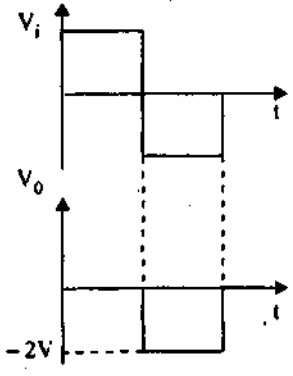
$$\Rightarrow \quad V_0 = 0$$

In negative cycle Diode is reverse biased and acts as open circuit but discharge time constant is very high. So negative maintains it's voltage during whole negative half cycle.



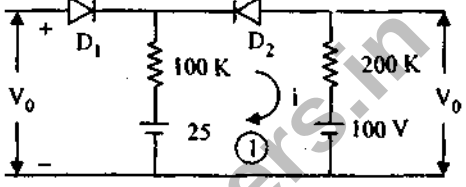
$$-V - V - V_0 = 0$$

$$\Rightarrow \boxed{V_0 = -2V}$$



Q. 7. (b) The input voltage V_i to the two level clipper shown in figure varies linearly from 0 to 150 V. Sketch and determine the output voltage V_0 to the same time scale as the input voltage. Assume ideal diodea.

Ans. when $0 < V_i < 25$



then D_1 off and D_2 on applying KVL in i

$$-200\,i - 100\,i - 25 + 100 = 0$$

$$i = \frac{75}{300} = \frac{1}{4}\text{ mA}$$

So $V_0 = 100 - i \times 200\text{ K}$

$$= 100 - \frac{1}{4}\text{ mA} \times 200\text{ K}$$

$$V_0 = 50\text{ V}$$

(ii) When $25 < V_i < 100$

D_1 On, D_2 On

So $V_0 = V_i$

(iii) When $100 < V_i < 150$

D_1 On, D_2 Off

So $V_0 = 100$ V