B.Tech.

SECOND SEMESTER EXAMINATION, 2009-10

ELECTRONICS ENGINEERING

(EEC-101/201)

Time : *3 Hours]* *[Total Marks : 100*

Note : *Attempt ALL questions.*

SECTION-A

Attempt all parts of this qnestion. All parts of the question carry equal marks.

Q. 1. This question contains 10 objective type/fill in the blank type/true-false type questions. Select most appropriate option **(10 × 2 = 20)**

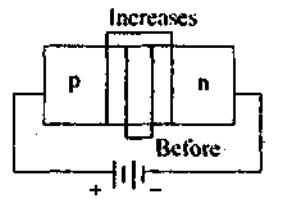
(a) When we apply reverse bias to a junction diode, it

(i) lowers the potential barrier.

(ii) raises the potential barrier.

(iii) greatly decreases the minority-carrier current.

(iv) greatly increases the majority-carrier current.



Ans. (ii) raises the potential barrier.

Hint :

(h) Ripple frequency of the ontput wave form of a full-wave rectifier when fed with a 50 Hz sine wave is :

(i) 25 Hz (il) 50 Hz (iii) 100 Hz (iv) 200 Hz

Ans. 100

. (c) "An ordinary transistor is called 'Blpolar Junctiou Transistor' because it has two polcs-one positive and the other negative". The statement is :

(i) True (ii) False

Ans. (ii) False. Hints : In bipolar function Transistor the conduction happen by both electron and hole. So it is call bipolar Transistor.

(d) The transistor configuration which provides highest output impedance is :

(i) Common Base (ii) Common Emitter

(iii) Common Collector (iv) None of the above

Ans. (i) Common Base

(e) In a Field Effect Transistor (FET) the gate to source voltage that gives zero drain curreut is called _____ voltage.

Ans. Pinch-ff

(f) When the positive voltage on the gate of a p-channel JFET is increased, its drain current :

(i) increases (il) decreases

(iii) remains the same (lv) none of the above

Ans. (i) increases.

(g) For the circuit shown in Figure-1., the output voltage v_0 is given by :

(i) $v_0 = -\frac{1}{RC}\frac{dv_i(t)}{dt}$ (ii) $v_0 = -\frac{1}{RC}\int_0^t v_i(t)\,dt$

(iii) $v_0 = -RC\frac{dv_i(t)}{dt}$ (iv) $v_0 = -RC\int_0^t v_i(t)\,dt$

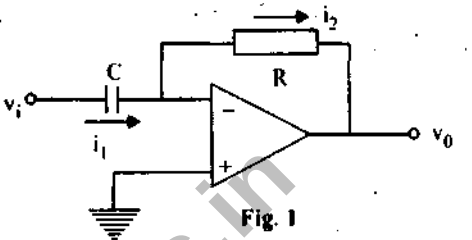


Fig. 1

Ans. (iii) $v_0 = -RC\frac{dv_i(t)}{dt}$. **Hints :** it is the circuit diagram of differentiator.

(h) Three Boolean operators are :

(i) NOT, OR, AND (ii) NOT, NAND, OR (iii) NOR, OR, NOT (iv) NOR, NAND, NOT

Ans. (i) NOT, OR, AND.

(i) Lissajous pattern obtained on the screen of a CRO can be used to determine:

(i) Phase shift **(ii) Amplitude distortion**

(iii) Voltage amplitude **(iv) None of the above.**

Ans. (iv) None of the above.

(j) "A digital voltmeter has negligible loading effect on the circuit under test because its input resistance is very high". The above statement is :

(i) True (ii) False

Ans. True.

SECTION-B

Q. 2. Attempt any three parts of the following : **(3 × 10 = 30)**

(a) (i) Describe the conditions established by forward and reverse-bias conditions on a p-n junction diode and how the resulting current is affected.

Ans. (i) Forward-Biasing of PN-junction: In forward-biasing of a PN-junction, positive terminal of the battery is connected to the P-side and the negative terminal to the N-side as shown in the figure. In this case, holes are repelled from the positive terminal of the battery and forced towards the junction. Similarly electrons are repelled from the negative terminal of the battery and forced towards the junction. Because of this increased energy, some holes and electrons enter the depletion region. This reduces the potential barrier. Therefore, width of depletion region also reduces. As a result of this, more majority carriers diffuse across the junction. Hence, this causes a large current to flow across the junction.

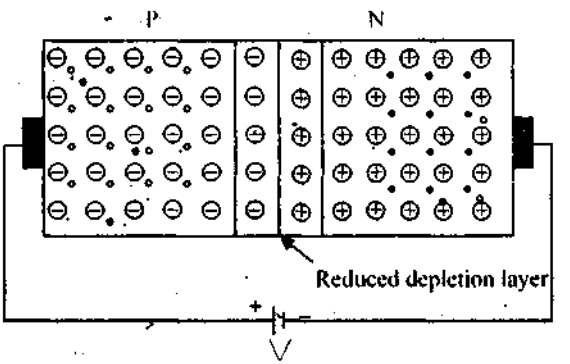


Fig. Forward biasing of PN-junction

Reverse Biasing of PN-Junction : In reverse biasing of a PN-junction, a battery is connected across the PN-junction in such a way

that its positive terminal is connected to the N-region and negative terminal is connected to the P-region.

In reverse bias the holes in the P-region are attracted towards the negative terminal of the battery whereas the electrons are attracted towards the positive terminal of the battery. In this way majority charge carriers are drawn away from the **PN-junction**. Due to this, the depletion region becomes wider.This increases the barrier potential.

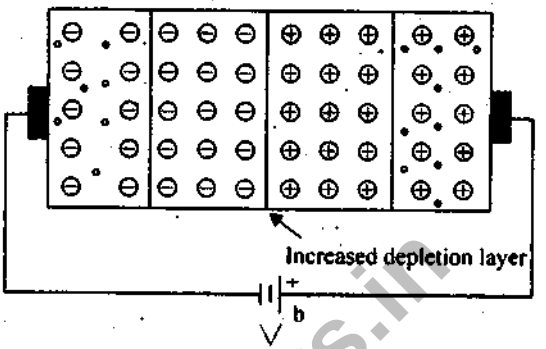


Fig. Reverse biasing of PN-junction

Due to the increased barrier potential, the majority charge carriers are not able to cross the junction. Hence, in reverse bias, there is no current due to the majority charge carriers.

Few Points :

(*i*) The characteristics curves show the three regions namely active region, cut-off region and saturation region.

(*ii*) In active region, the collector current is approximately equal to the emitter current I_E.

(*iii*) Emitter current increases slowly for increase in V_{CB} in active region. Hence, in active region, the curves are nearly flat. This also means that the output resistance in this configuration is very large.

(*iv*) If V_{CB} becomes negative, the collector-base junction is set in forward bias which causes collector current to decrease rapidly. This region is known as saturation region. In saturation region the collector current does not depend much on emitter current.

(*v*) In saturation region, since collector-base junction is also forward biased, a small increase in V_{CB} results in a large increase in collector current.

(*vi*) If emitter current I_E is made zero, then the collector current is not zero. It has a small value. This small value is leakage current I_{CBO}. The curve for $I_E = 0$ corresponds to cut-off region. In this region both the junctions are reverse-biased.

(*vii*) With the help of output characteristics,

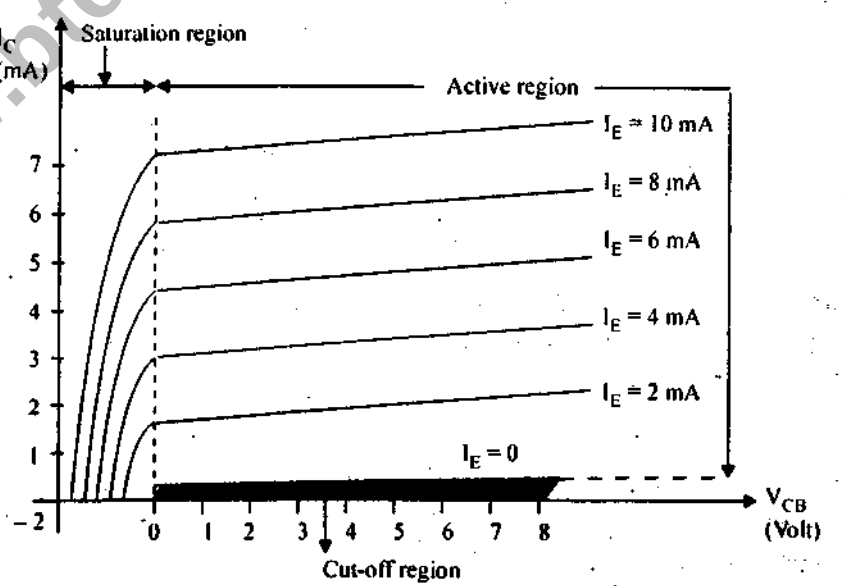


Fig. Output characteristics in a CB configurstion.

the dynamic output resistance r_0 can be found by the expression.

$$r_0 = \frac{\Delta V_{CB}}{\Delta I_C} \cdot I_E = \text{constant} \qquad ...(1)$$

Here ΔV_{CB} and ΔI_C are small changes in collector-to-emitter voltage and collector current for a given point.

(*viii*) With the help of output characteristics curve D.C. and A.C. current gains in CB configuration can also be determinad.

D.C. current gain

$$\alpha_{dc} = \alpha = \frac{I_C}{I_E} \qquad ...(2)$$

where I_C and I_E are the values of collector and emitter currents at any point on the curve. a.c. current gain is

Q. 2. (a) (ii) Calculate forward current I_F for the silicon dlode with dynamic resistance $r_d = 0.25\ \Omega$ used in the following circuit of Figure-2.

Ans. (ii)Applying KVL then we get

$1.5 - 10 \times I_F - 0.7 - 0.25 \times I_F = 0$

$1.5 - 0.7 = 10.25 I_F$

$I_F = \frac{0.8}{10.25} = 0.0780\ \text{A}$

$I_F = 78.0\ \text{mA}$

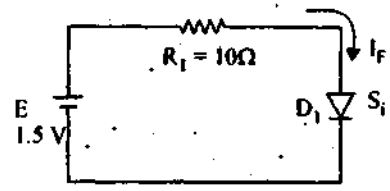
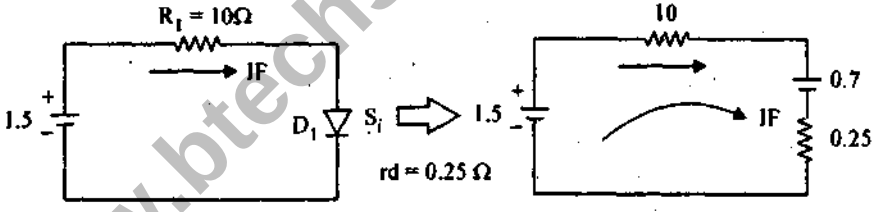


Fig. 2



Q. 2. (b) (i) What is tha major differenca betwean a hipolar and an unipolar device ? Explain with example.

Ans.

S.No.	Bipolar davica		Unipolar device
1.	In bipolar device the conduction happen by both electron and hole.	1.	In unipolar device the conduction happen by either electron or hole.
2.	BJT is example is the bipolar device.	2.	FET is example of unipolar device.

Q. 2. (b) (ll) Draw and explain the input aud output characteristics of common base configuration nsing npn bipolar junction transistor. Indicate all the region of operations.

Ans. ***Input characteristics in CB Configuration :***

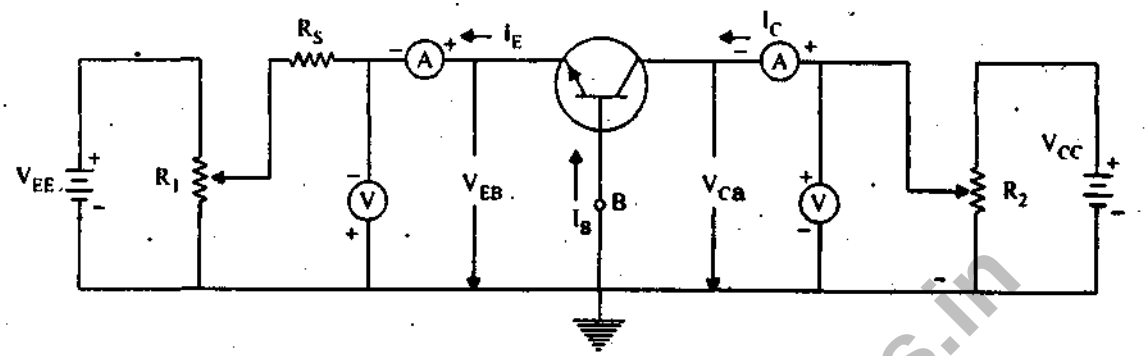


Fig. Circuit arrangement for input and output characteristics curve in CB configuration.

Input Characteristics Curves :

The input charecteristics in CB configuretion ere plotted between emitter current I_E and the emitter-base voltage V_{EB}, for different values of collector-base voltage V_{CB}. Input characteristice are shown in Figure.

Few Points :

(*i*) Below the cut-in voltege or knee voltege the emitter current is negligibly smell. This value of cut-in voltege is approximately 0.7V for silicon and 0.3V for germanium transistors.

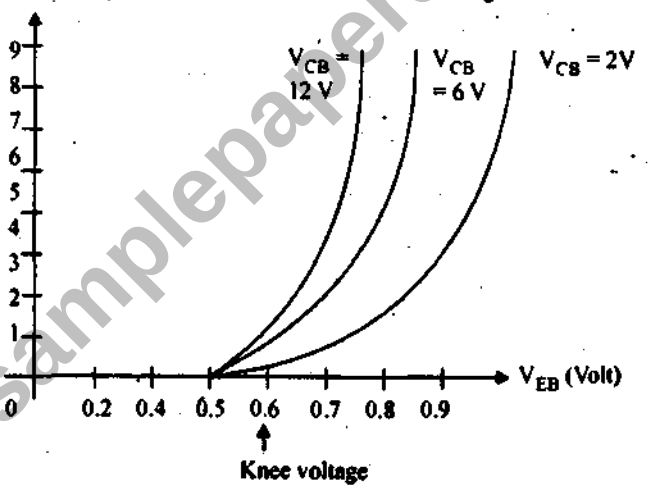


Fig. Input characteristics in CB configuration.

(*ii*) After the knee voltage the emitter current I_E increases rapidly with a small increese in emitter-to-base voltage V_{EB}. This indicates that resistence in *CB* configuration is very small.

(*iii*) With the increase in V_{CB}, the curves shift upwarda or becomes vertical. Hence, r_i decreeses.

(*iv*) At eny point on the curve, the value of e.c. or dynamic input resistance is given as

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} | V_{CB} = \text{constant}$$

where ΔV_{EB} → Small change in emitter-to-base voltage V_{EB}.

ΔI_E → Small change in emitter current I_E.

The dynemic input resistence r_i is very small nearly 25 to 100 Ω.

Q. 2. (c) (i) What are the advantage of FET over BJT. Explain.

Ans.

S.No.	Field-Effect Transistor (FET)	Bipolar junction transistor (BJT)
1.	It is an unipolar device *i.e.*, current in the device ia carried either by electrons or holes.	It is bipolar device, *i.e.*, current in the device is carried by both electrons and holes.

2.	It is a voltage-controlled device, *i.e.*, voltage at the gate (or drain) terminal controls the amount of current flowing through the device.	It is a current-controlled device, *i.e.*, the base current controls the amount of collector current.
3.	Its input resistence is very high and is of the order of several megaohms.	Ita input resistance is very low as compared to FET and is of the order of few kilo-ohms.
4.	It has a negative temperature coefficient at high current levels, It means that current decreases as the temperature increases. This characteristic prevents the FET from thermal breakdown.	It has a positive temperature coefficient at high current level, It means that collector current increases with the increase in temperature .This characteristic leads the BJT to thermal breakdown.
5.	It does not suffer from minority-carrier storage effects and therefore, has higher switching speeds and cut-off frequencies.	It suffers from minority carrier storage effects and therefore, has lower switching speed and cut-off frequencies than that of FET's.
6.	It is less noisy than a BJT or vacuum tube and is thus more suitable as an input amplifier for low-level signals. It is used extensively in high fidelity frequency modulated receivers.	It is comparatively more noisy than a field-effect transister.
7.	It is much simpler to fabricate as an integrated circuit (IC) and occupies a less apace of *IC* chip than that of BJT.	It is comparatively difficult to fabricate as an integrated circuit (IC) and occupies more space on IC chip than that of FET.

Q. 2. (c) (ii) Derive expressions for voltage gain of inverting and non-inverting ideal operational amplifier configurations.

Ans. Inverting amplifier :

At node *A* KCL

$I_1 = I_2 + I_3$, $I_2 = 0$, because the Ideal op-amp have Infinite impedance.

$I_1 = I_3$

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_0}{Rf}$$

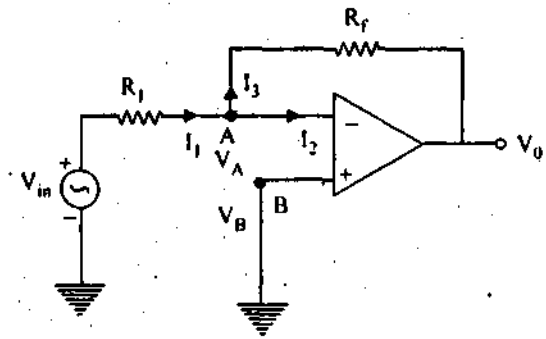
Using virtual ground concept

$V_A = V_B = 0$

$$\frac{V_{in} - 0}{R_1} = \frac{0 - V_0}{R_f}$$

$$\boxed{V_0 = -\frac{R_f}{R_1} . V_{in}}$$

From inverting amplifier



Applying KCL at Node A

$I_1 = I_2 + I_3$, $I_2 = 0$ because Ideal op-amp have infinite input impedance.

$I_1 = I_3$

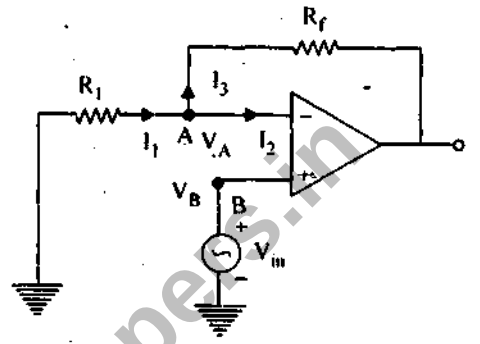
$$\frac{0 - VA}{R_1} = \frac{V_A - V_0}{R_f}$$

using virtual ground concept $V_A = V_B = V_{in}$

$$\frac{-V_{in}}{R_1} = \frac{V_{in} - V_0}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f}$$

$$\boxed{V_0 = \left(1 + \frac{R_f}{R_1}\right) V_{in}}$$

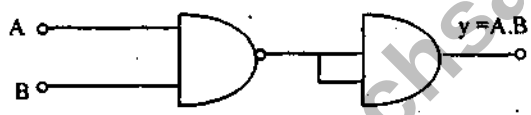


Q. 2. (d) (i) What are universai gates ? Why they are caiied so ? Justify your answer.

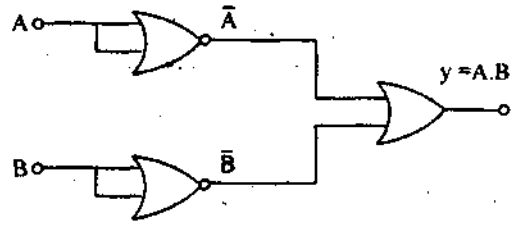
Ans. (i) NAND, and NOR Gate 18 called universal gate because they can be used as individually as the universal building block to build any logic circuit.

We can build any gate or any boolean expression by using universal gate.

ex. AND Gate using NAND Gate ,



AND Gate using NOR Gate



Q. 2. (d) (ii) What do yon underatand by don't care conditions ? Is it an advantage or disadvantage to include them in a map. Expiain with reasons.

Ans. For soap form, we enter 1's corresponding to the combination of input variables, which produce a high output. And we enter 0's in the remaining cells of the K map. For the POS form, we enter 0's corresponding to the combination of inputs which produce a low output and enter 1's in the remaining cells of the N-map.

But it is not always true that the cells not containing 1's (in SOP), will contain 0's, because some combination of input variables do not matter in such situation, we have a freedom to assume a 0 or 1 as output for each of these combinations. These conditions are known as the "Don't care conditions" and in the K-map, it represented as X (cross) mark in the corresponding all.

The don't care conditions (X) may be assumed to be 0 or 1 as per the need for simplification.

Q. 2. (e) Draw the hlock diagram of a CRO and hriefly explain the function of each hiock.

Ans. Block Diagram of C.R.O.

The block diagram of simple cathode ray oscilloscope is shown in fig.

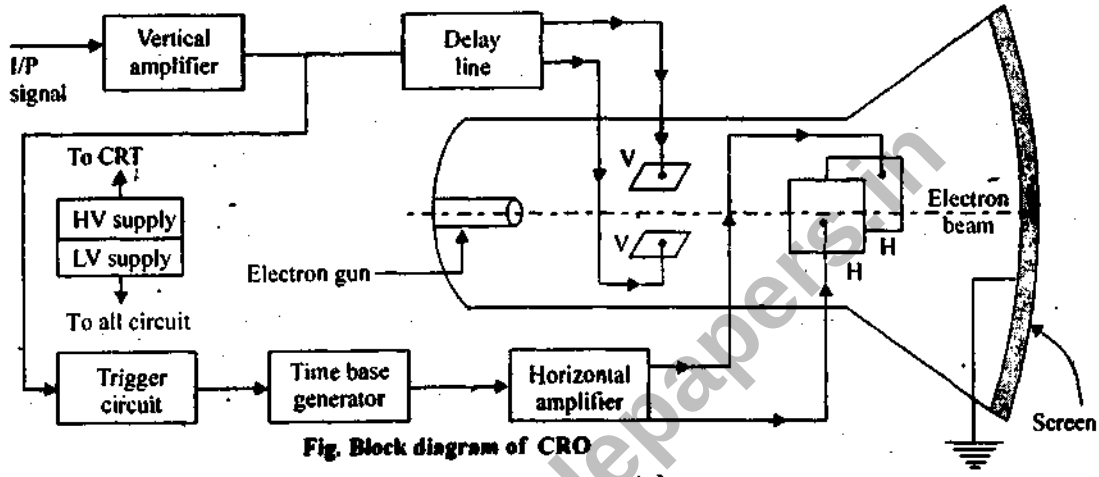


Fig. Block diagram of CRO

The main building blocks of C.R.O. are :

(1) The Cathode Ray Tube (CRT) (2) Vertical amplifier (3) Delay line

(4) Trigger circuit (5) Time base generator (6) Horizontal amplifier (7) Power supply.

Cathode Ray Tube (CRT) : It is Heart of CRO, the main working of CRO is to display the input voltage.

Vertical amplifier : The input voltage is applied to vertical amplifier, vertical amplifier amplifie the input voltage and delay line.

Delay line : The function of Delay lina is to provide the delay in input voltage. It is because to make synchronization between the o/p signal of vertical amplifier and o/p signal of horizontal amplifier.

Trigger Circuit : This circuit is used to provide Trigger pulse to Time base generator and Delay line.

Time base generator : Time base generator generate saw tooth pulse and apply these pulse to Horizontal amplifier.

SECTION-C

Attempt all questions. All questions carry equal marks. **(5 × 10 = 50)**

Q. 3. Attempt any two parts of the following : **(2 × 5 = 10)**

(a) Describe the physical mechanism of Zener breakdown. For the circuit shown in Figure-3, find the voltage drop across the 5 kΩ resistance.

Ans. Zener Breakdown : The zener breakdown is observed in the zener diodes having V_z less than 5 V or between 5 to 6 Volts. Let us understand the zener breakdown mechanism for V_z less than 5 V. When a reverse voltage (5V or less) is applied to a zener diode, it causes a vary intense electric field to appear across a narrow depletions region. The field intensity is typically of the order of 3×10^5 V/cm. Such an intense electric field is strong enough to pull some of the

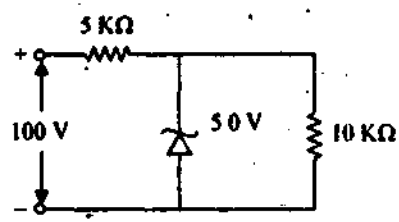


Fig. 3

valence electrons into the conduction band by breaking their covalent bonds. These electrons then become free electrons which are available for conduction. A large number of such free electrons will constitute a large reverse current through the zener diode and breakdown is said to have occurred due to the Zener effect.

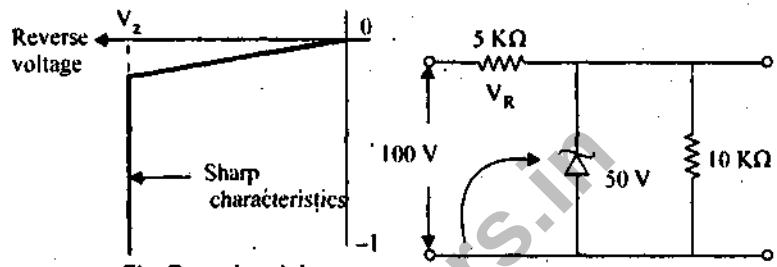


Fig. Zener breakdown

Applying KVL

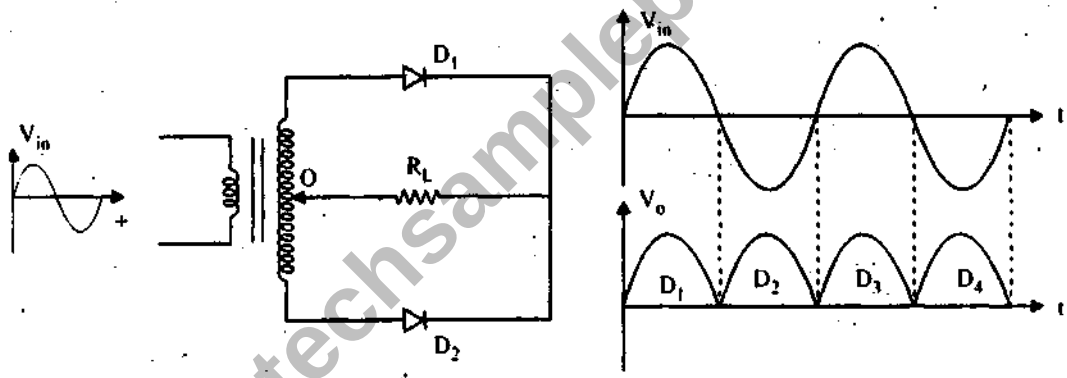
$100 - V_R - 50 = 0$

$\boxed{V_R = 50\ V}$

Voltage across the 5 kΩ Resistance is 5 kΩ is 50 V.

Q. 3. (h) Sketch a two-diode full wave rectifier circuit for producing a positive output voltage. Sketch the input and output waveforms and explain the circuit operation.

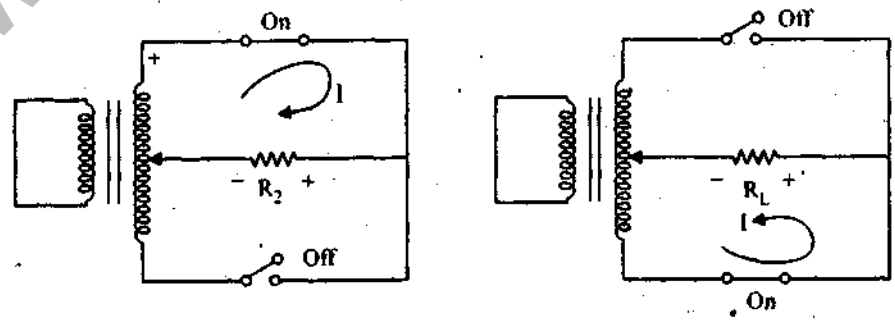
Ans. Two diode Full wave Rectifier :



In positive cycle :
D_1 diode will be on and
D_2 diode will be off.

In negative cycle :
D_1 diode will be off and
D_2 diode will be on

Q. 3. (c) Draw a voltage doubler circuit. Sketch input and output waveforms and explain the circuit operation.



Ans. Full-Wave Voltage Doubler : during the positive half cycle of a.c. input voltage, the diode D_1 conducts charging capacitor C_1 to a peak voltage V_m with polarity as shown in

figure. The diode D_2 is cut-off at this time, During the negative half-cycle, the diode D_2 conducts (while D_1 is at cut-off) charging capacitor C_2 to V_m. If there is no load connected across the output then the output voltage is equal to $2V_m$. However, if the load is connected then the voltage will be less than $2V_m$. The Peak Inverse Voltage (PIV) across each diode, in a full-wave voltage doubler is equal to $2V_m$. The full-wave voltage doubler has an advantage over a conventional center-tapped full wave rectifier that it does not require any center-tapped transformer.

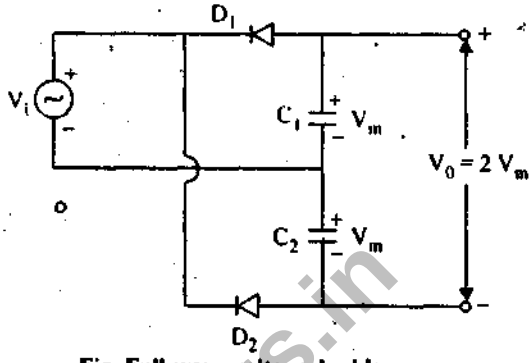


Fig. Full-wave voltage doubler.

Q. 4. Attempt any one of the following : **(1 × 10 = 10)**

Q. 4. (a) Derive the expressions for voltage gain, current gain and input impedance in terms of h-parameters for common emitter amplifier.

Ans.

(1) Current gain : The expression is

$$A_i = \frac{-h_f}{1 + h_o R_L}$$

for common emitter amplifier

$$A_i = \frac{-h_e}{1 + h_{oe} R_L}$$

$R_L \rightarrow$ load resistance

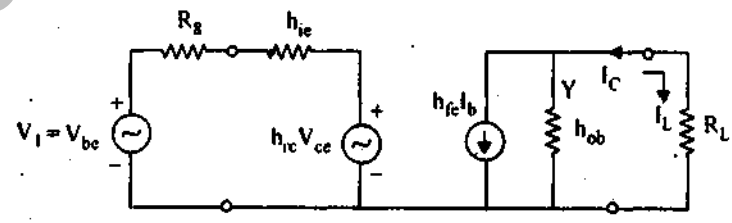
(2) Voltage gain : General expression

$$A_v = \frac{-h_f . R_L}{h_i + \Delta h . R_L}$$

for CE amplifier

$$A_v = \frac{-h_{fe} . R_L}{h_{ie} + \Delta h . R_L}$$

$$\Delta h = h_{ie} . h_{oe} - h_{re} . h_{fe}$$



(3) Input impedance :

General expression

$$R_L = h_i - \frac{h_r . h_f}{R_o + \frac{1}{R_L}}$$

$$\boxed{R_L = h_{ie} - \frac{h_{re} . h_{fe}}{h_{oe} + \frac{1}{R_L}}}$$

Hyhrid parameter :

$$V_{be} = h_{ie} + I_b + h_{re} . V_{ce} \quad ...(1)$$

$$I_c = h_{fe} . I_b + h_{oe} . V_{ce} \quad ...(2)$$

Q. 4. (b) Determine the following for the voltage divider bias circuit shown in Figure-4.

(i) I_C (ii) V_E (iii) V_B (iv) V_{CE} and (v) R_i.

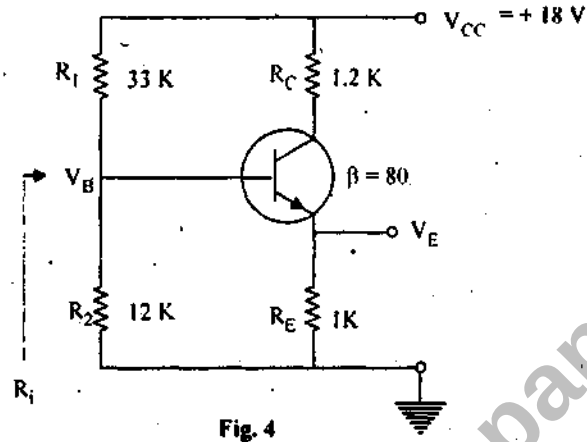


Fig. 4

Ans. $V_{CC} = +18\ V$

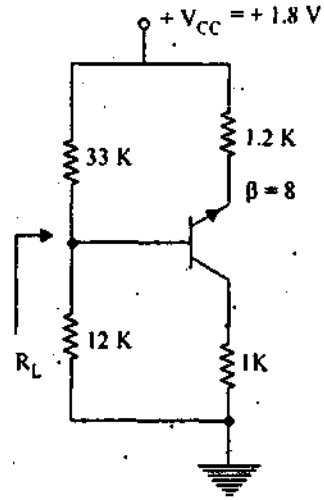
$$R_{th} = R_2 = \frac{33 \times 12}{12 + 33}$$

$$R_{th} = R_2 = 8.8\ k$$

$$V_{th} = \frac{18 \times 12}{33 + 12}$$

$$V_{th} = 4.8\ V$$

Thevenin equivalent chart



Applying KVL at loop (1)

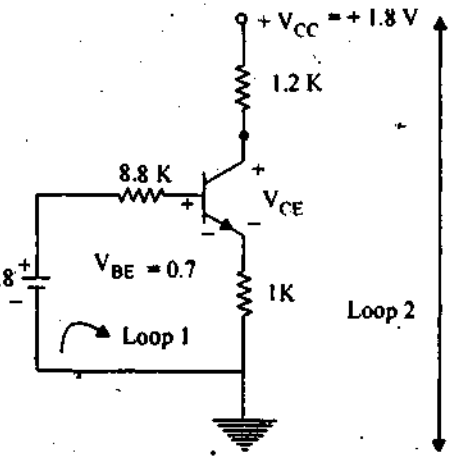
$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1 + R_B)\, R_E}$$

$$I_B = \frac{4.8 - 0.7}{8.8 + (80 + 1)\,1}$$

$$I_B = \frac{4.1}{89.8}$$

$$\boxed{I_B = 45.6\ mA}$$

$$\boxed{I_C = 3.65\ mA}$$



Applying KVL at loop (2)

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = 18 - 3.65 \times 10^{-3}\,(1.2 \times 10^3 + 1 \times 10^3)$$

$$V_{CE} = 18 - 3.65 \times 10^{-3} \times 2.2 \times 10^3$$

$$V_{CE} = 18 - 3.65 \times 2.2$$

$$V_{CE} = 18 - 8.03$$

$$\boxed{V_{CE} = 9.97\ V}$$

$$V_E = I_E \times R_E$$

$$V_E = 3.65 \times 10^{-3} \times 1 \times 10^3$$

$$\boxed{V_E = 3.65\ V}$$

$$V_B - V_{BE} - I_E R_E = 0$$

$$V_B = 0.7 + 3.65$$

$$\boxed{V_B = 4.35\ V}$$

Q. 5. Attempt any one of the following : **(1 × 10 = 10)**

Q. 5. (a) Deacribe the conatruction and operation of a MOSFET in enhancement mode. Draw its characteristics and equivalent circuit of the device.

Ans. MOSFET in enhancement mode : shows the drain characteristic for the N-channel depletion-type MOSFET in the common source configuration. These curves are plotted for both negative and positive values of gate-to-aource voltage (V_{GS}) . The curves shown above the curve for $V_{GS} = 0$ have a positive zero whera aa those below it have a negative value of V_{GS}. When V_{GS} is zero and negative, the MOSFET operates in the depletion-mode. On the other hand, if V_{GS} is zero and positive, the MOSFET operates in the enhancement-mode.

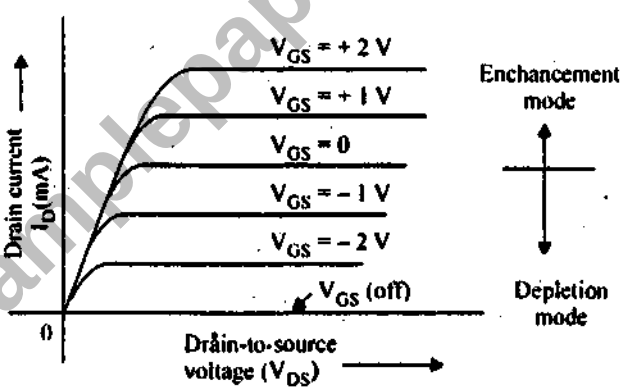


Fig. Drain characteristic of N-channel depletion-type MOSFET.

It may be noted that the drain characteristics of depletion-type MOSFETs are similar to that of JFET. The only difference is that JFET does not operate for positive values of gate-to-source voltage (V_{GS}).

Q. 5. (b) (i) Draw the circuit diagram for unity gain amplifier. Where is it used and why ?

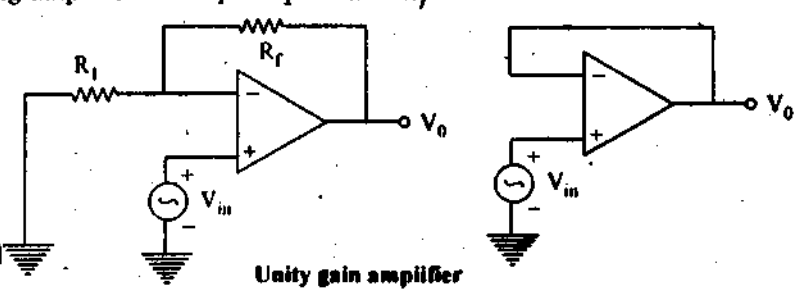
Ans. In the Non-inverting amplifier. It we put $R_1 = \infty$ and $R_f = 0$ than

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_{in}$$

$$V_0 = \left(1 + \frac{0}{\infty}\right) V_{in}$$

$$\boxed{V_0 = V_{in}}$$

Unit gain amplifier used as a buffer.



Unity gain amplifier

(ii) Find the output voltage of the following op-amp circuit show in Figure-5.

Ans. $V_0 = \frac{-R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) . V_2$

$$V_0 = -\frac{10\,k}{6\,k} \times V_1 + \left(1 + \frac{10\,k}{6\,k}\right)\left(\frac{1k}{5k + 1k}\right) . V_2$$

$$V_0 = -2V_1 + 3 \times \frac{1}{6} \times V_L$$

$$\boxed{V_0 = -2V_1 + 0.5\,V_2}$$

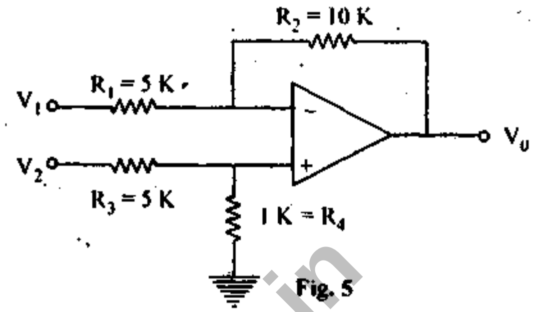


Fig. 5

Q. 6. Attempt any two of the following : **(2 × 5 = 10)**

Q. 6. (a) (i) Add and snbtract without converting the following two octal numbers 7461 and 3465.

(ii) Convert the following number as indicated :

(A) $(62.7)_6 = (\text{———})_{16}$ **(B)** $(BC\,64)_{16} = (\text{———})_{10}$ **(C)** $(111011)_2 = (\text{———})_5$

Ans. (i) Add the following Number $A = 7461$, $B = 3465$

Addition $A + B = 7461 + 3466 = 13146$

Subtraction $A - B = 7461 - 3465 = 3774$

(ii) (A) $(62.7)_8 = (\underset{2}{0010}\,\underset{A}{1010}.\underset{E}{1110})$

$$(62.7)_8 = (2\,A.\,E)_{16}$$

(B) $(B664)_{16} = 11 \times 16^3 + 12 \times 16^2 + 6 \times 10^1 + 4 \times 16^0$

$= (48228)_{10}$

(C) $(111011)_2 = (\text{———})_5 = (59)_{10} = (214)_5$

5	59	
5	11	4
6	2	1
	2	

Q. 6. (b) (i) Represent the unsigned decimal number 965 and 672 in BCD and then show the steps necessary to form their sum.

(ii) Express the Boolean function $F = xy + z$ in a product of max term form.

Ans. 965 → 1001 0110 0101 (in BCD)

672 → 0110 0111 0010 (in BCD)

1001	0110	0101	(in BCD)
0110	0111	0010	(in BCD)
+ 1111	1101	0111	(No carry)
16	3	7	

The sum will be (1637)

(ii) $F = xy + z$

Find 9 convert it into min term

$F = xy(z + \bar{z}) + (z(x + \bar{x})(y + \bar{y})$

$F = xyz + xy\bar{z} + z(xy + x\bar{y} + \bar{x}y + \bar{x}\,\bar{y})$

$F = xyz + xy\bar{z} + xyz + x\bar{y}z + \bar{x}yz + \bar{x}\,\bar{y}z$

Repeat

$F = xyz + xy\bar{z} + x\bar{y}z + \bar{x}yz + \bar{x}\,\bar{y}z$

we will get

$F = 111 + 110 + 101 + 011 + 001$

$F(x, y, z) = \Sigma m\,(1, 3, 5, 6, 7)$

The max term will be

$\boxed{F(x, y, z) = \Pi M\,(0, 2, 4)}$

Q. 6. (c) Given the Boolean function.

$F(A, B, C, D) =$

$\bar{A}\,\bar{B}\,\bar{C} + A\,\bar{C}\,\bar{D} + A\,\bar{B} + A\,B\,C\,\bar{D} + \bar{A}\,\bar{B}\,C$

(i) Express it in sum of minterms.

(ii) Find the minimal sum of products expression using K-map and implement the output using NAND gates only.

Ans. $F(A, B, C, D) = \bar{A}\bar{B}\bar{C} + A\bar{C}\,\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$

in Term of in term

$\bar{A}\bar{B}C\,(B + \bar{D}) = \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$

$A\bar{C}\bar{D}\,(B + \bar{B}) = A\,B\bar{C}\,\bar{D} + A\bar{B}\bar{C}\,\bar{D}$

$A\bar{B}(C + \bar{C})\,(D + \bar{D}) = A\bar{B}\,(CD + C\bar{D} + \bar{C}D + \bar{C}\,\bar{D})$

$= A\bar{B}CD + A\bar{B}\,C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\,\bar{D}$

$ABC\bar{D} = A\,BC\bar{D}$

$\bar{A}\,\bar{B}C\,(D + \bar{D}) = \bar{A}\,\bar{B}CD + \bar{A}\,\bar{B}C\,\bar{D}$

adding at the Term we will get

$= \bar{A}\bar{B}CD + \bar{A}\bar{B}\,C\bar{D} + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D}$

Repeat (1) Repeat (2) Repeat (3)

$+ A\bar{B}\bar{C}D + A\bar{B}\bar{C}\,\bar{D} + ABC\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$

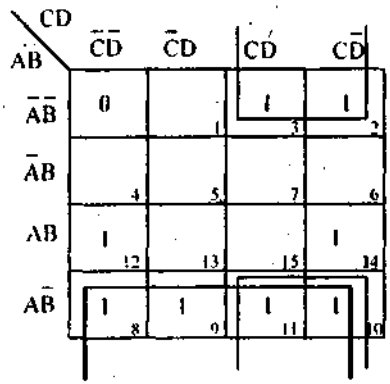
Repeat (3) Repeat (1) Repeat (2)

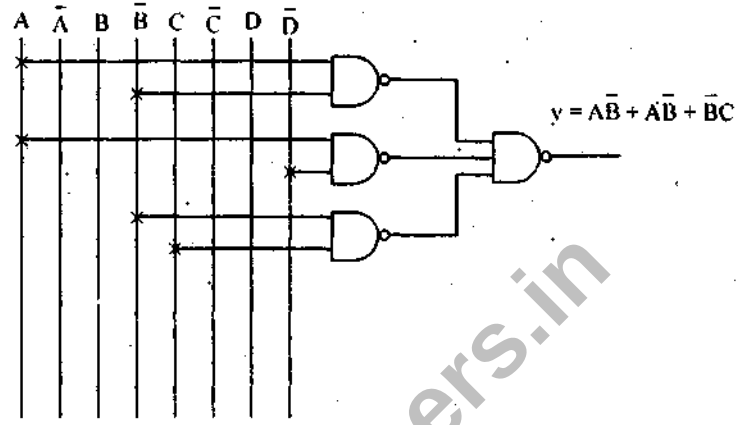
$= \bar{A}\bar{B}C\,D + \bar{A}\bar{B}C\,\bar{D} + ABC\,\bar{D} + A\bar{B}CD + A\bar{B}CD + A\bar{B}\bar{C}D + ABC\bar{D}$

convert into in is tem

$= 0011 + 0010 + 1100 + 1000 + 1011 + 1010 + 1001 + 1110$

$\Sigma F(A, B, C, D) = \Sigma m\,(2, 3, 8, 9, 10, 11, 12, 14)$





Q. 7. Attempt any one of the following : **(1 × 10 = 10)**

(a) Draw the Lissajous pattern you expect when the ratio of the frequency of the vertical input to that of the horizontal input is 1 : 2 Explain with the help of a neat diagram, why you get this pattern.

Ans. ***Basic circuit to obtain Lissajous figures :*** The basic circuit to measure frequency is shown in fig.

The know frequency is fed to horizontal deflecting plate. The unknown frequency is fed to vertical deflecting plate. The Lissajous pattern is obtained on the screen. The ratio is obtained from the horizontal tangencies and vertical tangencies.

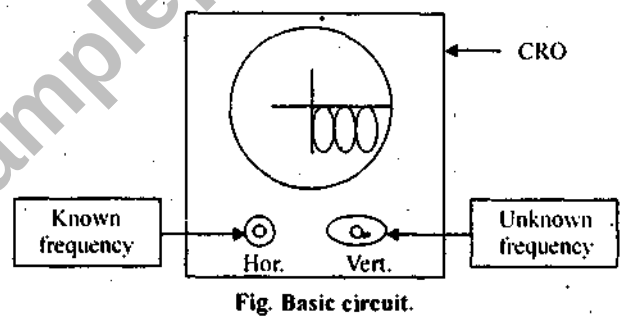


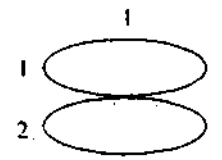
Fig. Basic circuit.

If frequency at vertical input and horizontal input a.c. 1 : 2 then

$$\frac{f_r}{f_h} = \frac{1}{2}$$

then Lissajous pattern will be

$$\frac{f_r}{f_h} = \frac{1}{2}$$



Pattern of Lissajous

Q. 7. (h) Explain briefly the working principle of a digital voltmeter. What are the advantages obtained by numeric read out ?

Ans. This type of ADC is called so because it uses a ramp generator to produce a time period that is proportional to the analog input voltage. The principle of operation is based on the measurement of time that a linear ramp voltage takes to change from the level of input voltage to zero voltage or vice-vers a. The time interval is measured with electronic time interval counter. The count is then displayed' as a number of digits on electronic indicating device.

The operating principle and block diagram or ramp type ADC are shown in figs. (a) and (b) respectively. Here we will discuss how ar analog voltage is measurd and converted into digital output.

(a) Position of first coincidence (Point A) : At the start, a ramp voltage is initiated. This voltage may be positive or negative but here we consider a negative going ramp voltage as shown in fig (a). The ramp voltage is continuously compared with the voltage to be meaaured. At the instant, when the ramp voltage becomes equal to the voltage becomes equal; to the voltage to the measured [point *A* in fig. (a)] the input comparator (coincidence circuit) generates a pulse. This pulse opens the gate shown in fig. (b).

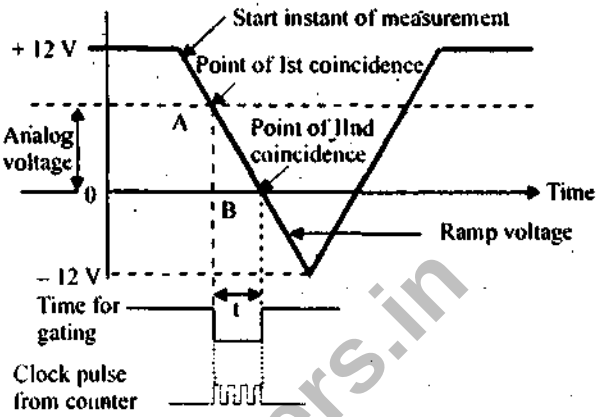


Fig. (a) Voltage to time conversion diagram.

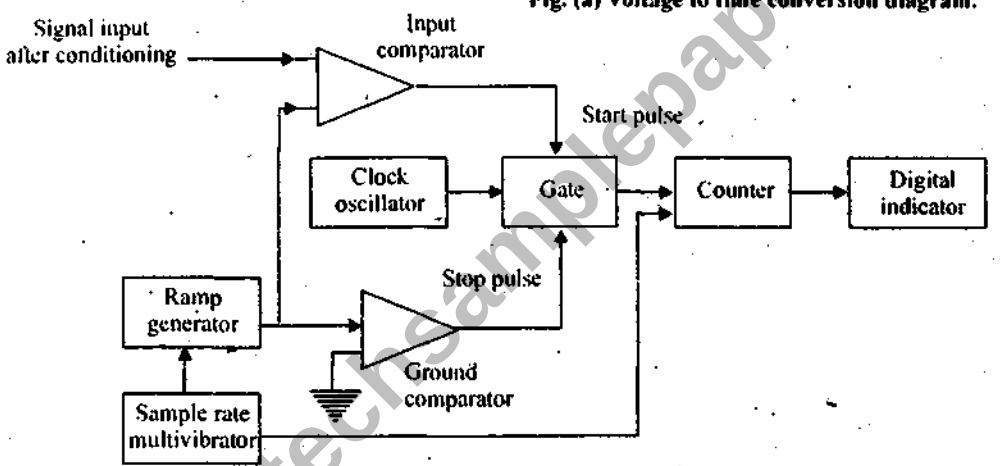


Fig. (b) Blockdiagram of ramp type ADC.

(b) Position of second coincidence (Point B) : It is obvious from fig. (a) that the ramp voltage continuously fall till it reaches a zero value as indicated by point *B*. At this instant, the ground compensator generates a stop pulse. The output stop pulse closes the gate. The stop pulse to gate is shown in fig. (b).

(c) Measurement of voltage : The time elapsed between opening and closing of the gate is *t*. The time duration of the gate opening is proportional to the value of the d.c. input voltage. During this time interval, pulses from a clock pulse oscillator passes through the gate. These pulses are counted and displayed. The decimal number indicated by the readout is a measure of input voltage. In this way an analog quantity (voltage) has been converted into a digital quantity. Analog to digital conversion process is now complete.

In Numeric readout we get the o/p in Numeric form, so it is easy to understand Numeric readout.